Chapter 16

MOSFET Digital Circuits

Chapter 16.1

NMOS Inverter

NMOS Inverter

- For any IC technology used in digital circuit design, the basic circuit element is the logic inverter.
- Once the operation and characterization of an inverter circuits are thoroughly understood, the results can be extended to the design of the logic gates and other more complex circuits.

MOSFET Digital Circuits

- In the late 70s as the era of LSI and VLSI began, NMOS became the fabrication technology of choice.
- Later the design flexibility and other advantages of the CMOS were realized, CMOS technology then replaced NMOS at all level of integration.
- The small transistor size and low power dissipation of CMOS circuits, demonstration principal advantages of CMOS over NMOS circuits.
NMOS Inverter

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- Once the operation and characterization of an inverter circuits are thoroughly understood, the results can be extended to the design of the logic gates and other more complex circuits.
NMOS Inverter

- If $V_{I} < V_{TN}$, the transistor is in cutoff and $i_D = 0$, there is no voltage drop across $R_D$, and the output voltage is $V_o = V_{DD} = V_{DS}$.

- If $V_{I} > V_{TN}$, the transistor is on and initially is biased in saturation region, since $V_{DS} < V_{GS} - V_{TN}$.

As the input voltage increases ($V_{GS}$), the drain to source voltage ($V_{DS}$) decreases and the transistor enters into the nonsaturation region.

NMOS Inverter with Resister Load

- If $V_{I} < V_{TN}$, the transistor is in cutoff and $i_D = 0$, there is no voltage drop across $R_D$, and the output voltage is $V_o = V_{DD} = V_{DS}$.

- As the input is increased slightly above the $V_{TN}$, the transistor turns on and is in the saturation region.

$$ V_{DD} \quad i_D \quad R_D \quad V_{DS} \quad V_{GS} \quad V_I \quad V_O = V_{DD} - V_{DS} $$

$$ i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{I} - V_{TN})^2 $$

$$ V_O = V_{DD} - K_n R_D (v_{I} - V_{TN})^2 $$

Saturation Region

- As the input voltage is further increased and voltage drop across the $R_D$ becomes sufficient to reduce the $V_{DS}$ such that $V_{BS} \leq V_{GS} - V_{TN}$, the $Q$-point of the transistor moves up the load line.

$$ V_{DS} \quad V_{GS} \quad V_{I} \quad V_O $$

$$ V_O = V_{DD} - V_{TN} $$

$$ V_{DS} \quad V_{GS} \quad V_{I} \quad V_O $$

$$ K_n R_D (V_{I} - V_{TN})^2 + (V_{I} - V_{TN}) - V_{DD} = 0 $$

Transition Region

Cut-off

- If $V_{I} < V_{TN}$, the transistor is in cutoff and $i_D = 0$, there is no voltage drop across $R_D$, and the output voltage is $V_o = V_{DD} = V_{DS}$.
As the input voltage becomes greater than $V_{th}$, the Q-point continues to move up the load line, and the transistor becomes biased in the nonsaturation region.

\[
\begin{align*}
  i_D &= K_n \left[ 2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2 \right] \\
  v_G &= V_{DD} - i_D R_D
\end{align*}
\]

The sharpness of the transition region increases with increasing load resistance.

The minimum output voltage, or the logic 0 level, for a high input decreases with increasing load resistance.

For the NMOS inverter shown in Fig. $V_{DD} = 3V$. Assume transistor parameters of $K_n = 60 \mu A/V^2$, W/L = 5, and $V_{TN} = 0.5 V$. (a) Find the value of $R_D$ such that $v_o = 0.1 V$ when $v_I = 3 V$. (b) Using the results of part (a) determine the transition point for the driver transistor.
n-Channel MOSFET connected as saturated load device

- An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter.
- Since the gate and drain of the transistor are connected, we have $V_{GS} = V_{DS}$ when $V_{GS} = V_{DS} > V_{TN}$, a non-zero drain current is induced in the transistor and hence the transistor operates in saturation only. And following condition is satisfied.

$$V_{DS} > (V_{GS} - V_{TN})$$

In the saturation region the drain current is

$$i_D = K_n(V_{GS} - V_{TN})^2 = K_n(V_{DS} - V_{TN})^2$$

The $i_D$ versus $v_{DS}$ characteristics are shown in Figure 16.7(b), which indicates that this device acts as a nonlinear resistor.

NMOS Inverter with Enhancement Load

- This basic inverter consists of two enhancement-only NMOS transistors.
- Much more practical than the resistor loaded inverter, because the resistors are thousand of times larger size than a MOSFET.

For $v_{DS} = v_{DS} \leq V_{TN}$, the drain-current is zero.

$$v_{DS} = v_{DS} > V_{TN}$$, a non-zero drain current is induced in the device.

$$v_{DS} = (v_{DS} - V_{TN}) = v_{DS}$$

$$i_D = K_n(V_{GS} - V_{TN})^2 = K_n(V_{DS} - V_{TN})^2$$

A transistor with this connection always operates in the saturation region when not in cutoff.
When $v_I < V_{TND}$, the driver is cut off and the drain currents are zero.

\[ i_{DL} = 0 = K_L(v_{DSL} - V_{TNL})^2 \]

\[ v_{DSL} = V_{DD} - V_T \]

\[ v_{DSL} - V_{TNL} = V_{DD} - v_0 - V_{TNL} = 0 \]

For the enhancement-load NMOS inverter, the maximum output voltage, which is the logic 1 level, does not reach the full $V_{DD}$ value.

When $v_I > V_{TND}$, the driver transistor turns on and is biased in the saturation region.

Two drain currents are equal since the output will be connected to the gates of other MOS transistors.

\[ K_D(v_{GSD} - V_{TND})^2 = K_L(v_{GSL} - V_{TNL})^2 \]

\[ K_D(v_I - V_{TND}) = K_L(v_{DD} - v_0 - V_{TNL})^2 \]

As the input voltage increases, the driver $Q$-point moves up the load curve and the output voltage decreases linearly with $v_I$.

At the driver transition point,

\[ V_{DS}(sat) = v_{GSD} - V_{TND} \quad \text{or} \quad V_{DS} = V_T - V_{TND} \]

\[ V_{DD} - V_{TNL} + V_{TNL} \left( 1 + \frac{K_D}{K_L} \right) \]

\[ V_{B} = \frac{K_D}{K_L} \left( V_{DD} - V_{TNL} - \frac{K_D}{K_L} (v_I - V_{TND}) \right) \]

\[ v_0 = V_{DD} - V_{TNL} - \frac{K_D}{K_L} (v_I - V_{TND}) \]
The sharpness of the transition region increases with increasing load resistance.

The minimum output voltage, or the logic 0 level, for a high input decreases with increasing load resistance.

As the width-to-length ratio of the load transistor decreases, the effective resistance increases.

The minimum output voltage, or the logic 0 level, for a high input decreases with an increasing $K_0/K_L$ ratio.

Voltage transfer characteristics, NMOS inverter with saturated load, for three aspect ratios

Voltage transfer characteristics, NMOS inverter with enhancement load, for three aspect ratios

The input-output relationship.

Example: Design the aspect ratio $K_0/K_L$ to produce a specified low output voltage, and determine the power dissipation in the inverter with enhancement load for a minimum $W/L$ ratio for the load transistor. (Neglect the body effect.)

Consider the inverter shown in Figure 16.8(a) biased at $V_{DD} = 5$ V. The transistor parameters are: $V_{TH0} = V_{THL} = 0.8$ V and $k'_0 = 35 \mu A/V^2$. Determine $K_0/K_L$ such that $v_0 = 0.10$ V when $v_I = \text{Logic 1} = 4.2$ V, and determine $(W/L)_b$ and the power dissipation in the inverter for $(W/L)_b = 0.5$ and $v_I = 4.2$ V.

Restoring logic

Logic signals that are degraded in one circuit can be restored by the gain of subsequent logic circuits.
Example

The enhancement-load NMOS inverter shown in Fig. is biased at $V_{DD} = 3$ V. The transistor parameters are $V_{TND} = V_{TNL} = 0.4$ V, $k' = 60$ mA/V², $(W/L)_D = 16$ and $(W/L)_L = 2$. (a) Find $v_o$ when (i) $v_I = 0$, (ii) $v_I = 2.6$. (b) Calculate the power dissipated in the inverter when $v_I = 2.6$ V.
NMOS Inverter with Depletion Load

Depletion mode: Channel exists even with zero gate voltage.
A negative voltage must be applied to the gate to turn the device off.
Threshold voltage is always negative.

This is an alternate form of the NMOS inverter that uses a depletion-mode MOSFET load device with gate and source terminal connected.

This inverter has the advantage of $V_O = V_{DD}$, as well as more abrupt transition region even though the $W/L$ ratio for the output MOSFET is small.

Depletion mode:
Channel exists even with zero gate voltage.

A negative voltage must be applied to the gate to turn the device off.
Threshold voltage is always negative.

This inverter has been the basis of many microprocessor and static memory designs.

Gate and source are connected, $V_{GSL} = 0$

Since the threshold voltage of load transistor is negative.

$V_{DSL}(Sat) = V_{GSL} - V_{TNL} = -V_{TNL}$

$V_{GSL} = 0$

NMOS Inverter with Depletion Load

N-Channel Depletion-Mode MOSFET

- In n-channel depletion mode MOSFET, an n-channel region or inversion layer exists under the gate oxide layer even at zero gate voltage and hence term depletion mode.
- A negative voltage must be applied to the gate to turn the device off.
- The threshold voltage is always negative for this kind of device.
NMOS Inverter with Depletion Load (cont.)

Case I: when \( V_I < V_{TND} \) (drive is cutoff): No drain current conduct in either transistor. That means the load transistor must be in the linear region of the operation and the output current can be expressed as fellows

\[ i_{DL(\text{linear})} = K_L \left[ 2(V_{GS} - V_{TND})V_{DSL} - V_{DSL}^2 \right] \]

Since \( V_{GS} = 0 \), and \( i_{DL} = 0 \)

\[ 0 = K_L \left[ 2V_{TND}V_{DSL} + V_{DSL}^2 \right] \]

Which gives \( V_{DSL} = 0 \) thus

\[ V_O = V_{DD} \]

This is the advantage of the depletion load inverter over the enhancement load inverter.

\[ \text{NMOS Inverter with Depletion Load} \]

\[ \text{transition point for the driver} \]

\[ V_{DS} = V_{GSD} - V_{TND} \]

\[ V_{DS} = V_{GSL} - V_{TNL} \]

When the Q-point lies between points B and C both devices are in the saturation region.

\[ K_D (V_{GSD} - V_{TND})^2 = K_L (V_{GSL} - V_{TNL})^2 \]

\[ K_D (V_I - V_{TND}) = -V_{TNL} \]

This implies that input voltage is constant as the Q-point passes this region.
**NMOS Inverter with Depletion Load**

Voltage transfer characteristics, NMOS inverter with depletion load,

Example 16.4 **Objective:** Design the aspect ratio $K_D/K_L$ to produce a specified low output voltage, and determine the power dissipation in the inverter with depletion load for a minimum $W/L$ ratio for the load transistor.

Consider the inverter in Figure 16.10(a) biased at $V_{DD} = 5$ V. The transistor parameters are: $V_{PDT} = 0.8$ V, $V_{PNT} = -2$ V, and $K'_p = 35 \mu A/V^2$. Determine $K_D/K_L$ such that $V_T = 0.10$ V when $\gamma = 5$ V. Determine $(W/L)_D$ and the power dissipation in the inverter for $(W/L)_L = 0.5$.

For $\gamma = 5$ V, we assume the driver transistor is in the non-saturation region.

\[
\frac{K_D}{K_L} = \frac{1}{k_p} \left( 2(1 - V_{TNO})_D - V_T \right) = \frac{1}{35} \left( -1 \right) = -0.0286
\]

\[
\frac{K_D}{K_L} = \frac{2(5 - 0.8)(0.1) - (0.1)^2}{(-2)^2} = 4.82
\]

For $(W/L)_D = 2.41$ when $(W/L)_L = 0.5$ from the load transistor,

\[
V_T = K_D(V_{PNT})^2 = \frac{k_p'}{2} \left( \frac{W}{L} \right) (V_{PNT})^2 = \frac{35}{2} \times 0.5 = 87.5 \mu A
\]

The power dissipated in the inverter is $P = \alpha V_{DD} = (35)(5) = 175 \mu W$.
**Example 16.4**  
**Objective:** Design the aspect ratio $K_D/K_L$ to produce a specified low output voltage, and determine the power dissipation in the inverter with depletion load for a minimum $W/L$ ratio for the load transistor.

Consider the inverter in Figure 16.10(a) biased at $V_{DD} = 5$ V. The transistor parameters are: $V_{THD} = 0.8$ V, $V_{THN} = -2$ V, and $K'_s = 35$ $\mu$A/V$^2$. Determine $K_D/K_L$ such that $V_O = 0.10$ V when $V_T = 5$ V. Determine $(W/L)_D$ and the power dissipation in the inverter for $(W/L)_L = 0.5$.

**Current-Voltage Relationship**

**Saturation Region**

$$i_D = K_D(v_{GS} - V_{TN})^2 = K_D(v_T - V_{TN})^2$$

$$v_O = V_{DD} - K_D v_T (v_T - V_{TN})$$

**Transition Region**

$$V_{OH} = V_T - V_{TN}$$

$$K_D R_D (v_T - V_{TN})^2 + (V_T - V_{TN}) - V_{DD} = 0$$

**Nonsaturation Region**

$$i_D = K_D [2(v_T - V_{TN})v_O - v_O^2]$$

$$v_O = V_{DD} - K_D R_D [2(v_T - V_{TN})v_O - v_O^2]$$

**Design Example 16.5**  
**Objective:** Design the aspect ratio $K_D/K_L$ to produce a specified low output voltage, and determine the power dissipation in the inverter with depletion load for a minimum $W/L$ ratio for the load transistor.

Consider the inverter in Figure 16.10(a) biased at $V_{DD} = 5$ V. The transistor parameters are: $V_{THD} = 0.8$ V, $V_{THN} = -2$ V, and $K'_s = 35$ $\mu$A/V$^2$. Determine $K_D/K_L$ such that $V_O = 0.10$ V when $V_T = 5$ V. Determine $(W/L)_D$ and the power dissipation in the inverter for $(W/L)_L = 0.5$.

**Comment:** A relatively low output voltage $V_{OL}$ can be produced in the NMOS inverter with depletion load, even when the load and driver transistors are not vastly different in size. The power dissipation in this inverter is also substantially less than in the enhancement-load inverter since the aspect ratio is smaller.
Design 16.5 Consider the depletion load inverter in Figure 16.10(a) biased at $V_{DD} = 5 \text{ V}$. The threshold voltages are $V_{TH} = 0.8 \text{ V}$ and $V_{PM} = -2 \text{ V}$. Design the inverter such that the maximum power dissipation is 350 $\mu$W and the output voltage is 0.05 V when $v_I = 5 \text{ V}$. (Ans. $W/L_p = 1, (W/L)_D = 9.58$)

\[ P = I_D V_{DD} \]
\[ 350 = I_D 5 \Rightarrow I_D = 70 \times 10^{-6} \text{ A} \]
\[ I_D = 70 \times 10^{-6} \text{ A} \] (Load)

Since Gate to Source terminal of $Q_2$ (load transistor) are short
\[ V_{SS} = 0 \text{ V}, \text{ which is much greater than } V_{TH} \]

Load transistor is in Saturation mode
\[ I_D = K_D (V_{GS} - V_{TH})^2 \]
\[ I_D = K_D (V_{GS} - V_{TH})^2 = \frac{K_D}{2} (V_{GS} - V_{TH}) \]
\[ I_D = \frac{K_D}{2} (V_{GS} - V_{TH}) \]
\[ 70 = \frac{K_D}{2} (V_{GS} - V_{TH}) \]
\[ 70 = 7 \times 10^{-6} \times (V_{GS} - V_{TH}) \]
\[ (V_{GS})_D = 9.58 \text{ V} \]

Example 16.14 Calculate the power dissipated in each inverter circuit in Figure P16.14 for the following input conditions: (a) Inverter a: (i) $v_I = 0.5 \text{ V}$, (ii) $v_I = 5 \text{ V}$; (b) Inverter b: (i) $v_I = 0.25 \text{ V}$, (ii) $v_I = 4.3 \text{ V}$; (c) Inverter c: (i) $v_I = 0.03 \text{ V}$, (ii) $v_I = 5 \text{ V}$.

16.14  Calculate the power dissipated in each inverter circuit in Figure P16.14 for the following input conditions: (a) Inverter a: (i) $v_I = 0.5 \text{ V}$, (ii) $v_I = 5 \text{ V}$; (b) Inverter b: (i) $v_I = 0.25 \text{ V}$, (ii) $v_I = 4.3 \text{ V}$; (c) Inverter c: (i) $v_I = 0.03 \text{ V}$, (ii) $v_I = 5 \text{ V}$.

(i) $v_I = 0.5 \text{ V}$ \Rightarrow $I_D = 0 \Rightarrow P = 0$

(ii) $v_I = 5 \text{ V}$, From Equation (16.12),

\[ v_o = V_{DD} - K_i R \left[ 2(5 - 1.5) v_o - v_0 \right] \]

\[ v_o = 5 - (0.1)(20)[2(5 - 1.5)v_o - v_0] \]

\[ v_o = 5 - 20 = 0 \]

\[ v_o = 0.35 \text{ V} \]

\[ i_D = \frac{5 - 0.35}{20} = 0.2325 \text{ mA} \]

\[ P = i_D \cdot V_{DD} = (0.2325)(5) \Rightarrow P = 1.16 \text{ mW} \]
Example 16.14 Calculate the power dissipated in each inverter circuit in Figure P16.14 for the following input conditions: (a) Inverter at (i) $v_I = 0.5\text{ V}$; (ii) $v_I = 5\text{ V}$; (b) Inverter b: (i) $v_I = 0.25\text{ V}$; (ii) $v_I = 4.3\text{ V}$; (c) Inverter c: (i) $v_I = 0.03\text{ V}$; (ii) $v_I = 5\text{ V}$.

(i) $v_I = 0.25\text{ V}$ \Rightarrow $i_D = 0 \Rightarrow P = 0$

(ii) $v_I = 4.3\text{ V}$; From Equation (16.23), input voltage greater than $V_T$:

\[ K_D [2(v_I - V_{TNO})v_O - v_I^2] = K_L (V_{DD} - v_O - V_{TNE})^2 \]

\[ 100 [2(4.3 - 0.7)v_O - v_I^2] = 10[5 - v_O - 0.7]^2 \]

\[ 10 [7.2v_O - v_I^2] = 18.45 - 8.6v_O + v_O^2 \]

\[ 11v_O^2 - 80.6v_O + 18.49 = 0 \]

\[ v_O = \frac{-80.6 \pm \sqrt{(80.6)^2 - 4(11)(18.49)}}{2(11)} \approx 0.237 \text{ V} \]

\[ i_D = 10(5 - 0.237 - 0.7)^2 = 155 \text{ µA} \]

\[ P = i_D \cdot V_{DD} = (155)(5) \Rightarrow P = 825 \text{ µW} \]

(c) $V_{DD} = 1\text{ V}$

\[ i_D = K_L (-v_{TNE})^2 = (10)(-2)^2 = 40 \text{ µA} \]

\[ P = i_D \cdot V_{DD} = (40)(5) \Rightarrow P = 200 \text{ µW} \]

Chapter 16

MOSFET Digital Circuits

Chapter 16.2

NMOS Logic Circuit
NMOS logic circuits are constructed by connecting driver transistor in parallel, series or series-parallel combinations to produce required output logic function.

NMOS NOR gate can be constructed by connecting an additional driver transistor in parallel with a depletion load inverter.

- If $A = B = \text{logic 0}$, then both $M_{DB}$ and $M_{DA}$ are cut off and $v_D = V_{DD}$.
- If $A = \text{logic 1}$ and $B = \text{logic 0}$, then $M_{DB}$ is cut off and the NMOS inverter with $M_L$ and $M_{DA}$.
- If $A = \text{logic 0}$ and $B = \text{logic 1}$, the same inverter configuration.

Logic Gates

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Two-input NMOS NOR logic gate with depletion load.
**NMOS NOR Gate**

If \( A = B = \text{logic 1} \), then both \( M_{DA} \) and \( M_{DB} \) turn on and the two driver transistors are effectively in parallel.

The value of the output voltage changes slightly:

\[ i_{DL} = i_{DA} + i_{DB} \]

\[ V_{DO} = \frac{K_D [\gamma_{DSL} - V_{T_{N1L}}]^2}{K_L [2(\gamma_{GSL} - V_{T_{N1A}})\gamma_{DSL} - \gamma_{T_{N1A}}]} \]

If transistors are identical,

\[ K_{DA} = K_{DB} = K_D \]

\[ V_{TN1A} = V_{TN1B} = V_{TNB} \]

\[ \gamma_{GSL} = 0, \gamma_{GSL} = \gamma_{GSR} = V_{DD}, \gamma_{DSL} = \gamma_{DSR} = V_{DO} \]

\[ (-V_{T_{N1L}})^2 = 2 \left( \frac{K_D}{K_L} \right) [2(V_{DD} - V_{TNB})V_{DO} - V_{DO}^2] \]

When both drivers are conducting, the effective width-length ratio of the composite driver transistor doubles, the output voltage becomes slightly smaller when both inputs are high.

**NMOS NOR Gate**

When all Inputs are at logic 1

When \( A = B = \text{logic 1} \), both driver transistors are switched into nonsaturation region and load transistor is biased in saturation region.

\[ i_{DL} = i_{DA} = i_{DB} \]

\[ K_D [\gamma_{GSL} - V_{T_{N1L}}]^2 = K_D \left[ 2(\gamma_{GSL} - V_{T_{N1A}})\gamma_{DSL} - \gamma_{T_{N1A}} \right] + 2K_D \frac{2(\gamma_{GSL} - V_{T_{N1B}})\gamma_{DSL} - \gamma_{T_{N1B}}}{\gamma_{GSL} - V_{T_{N1L}}} \]

Suppose two driver transistors are identical.

\[ K_{DA} = K_{DB} = K_D \]

\[ V_{TN1A} = V_{TN1B} = V_{TNB} \]

\[ \gamma_{GSL} = 0, \gamma_{GSL} = \gamma_{GSR} = V_{DD}, \gamma_{DSL} = \gamma_{DSR} = V_{DO} \]

\[ (-V_{T_{N1L}})^2 = 2 \frac{K_D}{K_L} [2(V_{DD} - V_{TNB})V_{DO} - V_{DO}^2] \]

When both drivers are conducting, the effective width-length ratio of the composite driver transistor doubles.

This means that the output voltage becomes slightly smaller when both inputs are high.

Higher the output stage lower the output.

---

**Example 16.7**

Objective: Determine the low output voltage of an NMOS NOR circuit.

Consider the NOR circuit in Figure 16.24 biased at \( V_{DD} = 5 \text{ V} \). Assume that \( K_d = 33 \mu \text{A/V}^2 \). Also assume the width-length ratios of the load and driver transistors are \( (W/L)_D = 4 \), respectively. Let \( V_{TND} = 0.8 \text{ V} \) and \( V_{TSL} = -2 \text{ V} \). Neglect the body effect.

\[ V_{DO} = \text{5 V} \]

If \( A = \text{logic 1} \) and \( B = \text{logic 0} \), then \( M_{DB} \) is cut off.

\[ \frac{K_D}{K_L} [2(\gamma_{V_{T_{N1A}}})V_{DO} - V_{DO}^2] = (-V_{T_{N1L}})^2 \]

\[ \frac{K_D}{K_L} [2(V_{DD} - V_{TNB})V_{DO} - V_{DO}^2] = (-V_{T_{N1L}})^2 \]

\[ \frac{K_D}{K_L} [2(V_{DD} - V_{TNB})V_{DO} - V_{DO}^2] = \left( \frac{4}{25} \right) [25 - 0.8V_{DO} - V_{DO}^2] = 0.121 \text{ V} \]

If both inputs go high,

\[ A = B = V_{DD} = 5 \text{ V} \]

\[ (-V_{T_{N1L}})^2 = 2 \left( \frac{K_D}{K_L} \right) [2(V_{DD} - V_{TNB})V_{DO} - V_{DO}^2] \]

\[ (-V_{T_{N1L}})^2 = 2 \left( \frac{K_D}{K_L} \right) [2(V_{DD} - V_{TNB})V_{DO} - V_{DO}^2] \]

\[ (25) = \left( \frac{4}{25} \right) [25 - 0.8V_{DO} - V_{DO}^2] \]

\[ V_{DO} = 0.060 \text{ V} \]

**NMOS NAND Gate**

Additional driver transistor connected in Series

If both \( A = B = \text{logic 0} \), or if either \( A \) or \( B \) is a logic 0, at least one driver is cut off, and the output is high.

If both \( A = B = \text{logic 1} \), then the composite driver of the NMOS inverter conducts, and the output goes low.

Since the gate-to-source voltages of \( M_{DA} \) and \( M_{DB} \) are not equal, determining the actual voltage \( V_{OL} \) of a NAND gate is difficult. The drain-to-source voltages of \( M_{DA} \) and \( M_{DB} \) must adjust themselves to produce the same current.
For the NOR gate the effective width of the drivers transistors doubles. The effective aspect ratio is increased.

For the NAND gate the effective length of the driver transistors doubles. The effective aspect ratio is decreased.

D16.20 Consider the three-input NOR logic gate in Figure P16.20. The transistor parameters are $V_{TN1} = -1\,\text{V}$ and $V_{TN2} = 0.5\,\text{V}$. The maximum value of $v_o$ in its low state is to be 0.1 V. (a) Determine $K_w/K_L$. (b) The maximum power dissipation in the NOR logic gate is to be 0.1 mW. Determine the width-to-length ratios of the transistors. (c) Determine $v_o$ when $v_T = v_T = v_T = 3\,\text{V}$.

\[
P = i_d \cdot V_{DD}
\]

\[
0.1 = i_d(3) \Rightarrow i_d = 333\,\mu A
\]

\[
i_d = \left(\frac{K_w}{K_L}\right) \left(\frac{W}{L}\right)_1 \left(\frac{V_{DD}}{L}\right)_1 \left(V_{TN1} \right)_1^3
\]

\[
333 = \left(\frac{80\,W}{2\,L}\right) \left(-1\right)^3 \Rightarrow \left(\frac{W}{L}\right)_1 = 0.8325
\]

\[
\left(\frac{W}{L}\right)_D = 1.70
\]

(a) Maximum value of $v_o$ in low state- when only one input is high, then

\[
k_w/k_L \left[2(3 - 0.5)v_o - 0.5\right] = \left(-1\right)^3 = 2.04
\]

\[
3(2.04)[2(3 - 0.5)v_o - v_o^3] = \left(-1\right)^3 \Rightarrow v_o = 0.0329\,\text{V}
\]
Fan-In and Fan-Out

- **Fan-in** of a gate is the number of its inputs. Thus a four input NOR gate has a fan-in of 4.
- Similarly, **Fan-Out** is the maximum number of similar gates that a gate can drive while remaining within guaranteed specifications.

Transient Analysis of NMOS Inverters

- The source of capacitance $C_{T1}$ and $C_{T2}$ are the transistor input capacitances and parasitic capacitances due to interconnect lines between the inverter stages.
- The constant current over a wide range of $V_{DS}$ provided by the depletion load implies that this type of inverter switch a capacitive load more rapidly than the other two types inverter configurations.

The rate at which the voltage across a load capacitance changes is a direct function of the current through the capacitance.

Chapter 16

MOSFET Digital Circuits

Chapter 16.3

CMOS Inverter
**p-Channel MOSFET**

In p-channel enhancement device, a negative gate-to-source voltage must be applied to create the inversion layer, or channel region, of holes that "connect" the source and drain regions.

The threshold voltage \( V_{TP} \) for p-channel enhancement-mode device is always negative and positive for depletion-mode PMOS.

**Summary of Transistor Operation**

<table>
<thead>
<tr>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nonsaturation region ( (V_{DS} &lt; V_{DS}\text{(sat)}) )</td>
<td>Nonsaturation region ( (V_{SD} &lt; V_{SD}\text{(sat)}) )</td>
</tr>
<tr>
<td>( i_D = K_d(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2) )</td>
<td>( i_D = K_d(2V_{GD} + V_{TP})V_{SD} - V_{SD}^2 )</td>
</tr>
<tr>
<td>Saturation region ( (V_{DS} &gt; V_{DS}\text{(sat)}) )</td>
<td>Saturation region ( (V_{SD} &gt; V_{SD}\text{(sat)}) )</td>
</tr>
<tr>
<td>( i_D = K_d(V_{GS} - V_{TH})^2 )</td>
<td>( i_D = K_d(V_{GD} + V_{TP})^2 )</td>
</tr>
<tr>
<td>Transition point ( V_{DS}\text{(sat)} = V_{GS} - V_{TH} )</td>
<td>Transition point ( V_{SD}\text{(sat)} = V_{GD} + V_{TP} )</td>
</tr>
<tr>
<td>Enhancement mode ( V_{TH} &gt; 0 )</td>
<td>Enhancement mode ( V_{TP} &lt; 0 )</td>
</tr>
<tr>
<td>Depletion mode ( V_{TH} &lt; 0 )</td>
<td>Depletion mode ( V_{TP} &gt; 0 )</td>
</tr>
</tbody>
</table>

**CMOS**

**Complementary MOS**

The most abundant devices on earth

- Although the processing is more complicated for CMOS circuits than for NMOS circuits, CMOS has replaced NMOS at all levels of integration, in both analog and digital applications.
- The basic reason for this replacement is that the power dissipation in CMOS logic circuits is much less than in NMOS circuits.
CMOS Properties

- Full rail-to-rail swing → high noise margins
  - Logic levels not dependent upon the relative device sizes → transistors can be minimum size → ratio less

- Always a path to $V_{DD}$ or GND in steady state → low output impedance (output resistance in kΩ range) → large fan-out.

- Extremely high input resistance (gate of MOS transistor is near perfect insulator) → nearly zero steady-state input current

- No direct path steady-state between power and ground → no static power dissipation

- Propagation delay function of load capacitance and resistance of transistors

CMOS Inverter

- In the fabrication process, a separate p-well region is formed within the starting n-substrate.
- The n-channel MOSFET is fabricated in the p-well region and p-channel MOSFET is fabricated in the n-substrate.

CMOS Inverter

**Steady State Response**

- $V_{OL} = 0$
- $V_{OH} = V_{DD}$

DC Analysis of the CMOS Inverter

Both transistors are enhancement-mode devices

For $V_L = 0$, the NMOS device is cut-off, $i_{GD} = 0$, and $i_{DP} = 0$, PMOS source-to-gate voltage is $V_{PD}$, PMOS is biased on the curve marked B
**DC Analysis of the CMOS Inverter**

For $V_D = 0$, the NMOS device is cut off. $i_{DS} = 0$, and $i_{DP} = 0$. PMOS source-to-gate voltage is $V_{GD}$. PMOS is biased on the curve marked B.

Since the only point on the curve corresponding to $i_{DP} = 0$ occurs at $v_{DS} = 0 = V_{DD} - V_D$, the output voltage is $V_O = V_D$. This condition exists as long as the NMOS transistor is cut off, or $v_D < V_{PD}$.

**Voltage Transfer Curve**

For $V_D = V_{PD}$, the PMOS device is cut off. $i_{DP} = 0$, and $i_{DN} = 0$. NMOS gate-to-source voltage is $V_{GS}$. NMOS is biased on the curve marked A. The only point on the curve corresponding to $i_{DN} = 0$ occurs at $v_{DS} = V_D = 0$. The output voltage is zero as long as the PMOS transistor is cut off $v_D < V_{PD}$

input voltage is in the range $V_{PD} - |V_{PP}| < v_D < V_{PD}$.

**DC Analysis of the CMOS Inverter**

CMOS inverter output voltage for input voltage in either high state or low state.
EX 16.2

(a) 

\[ v_a = V_{cc} - I_D R_D \]

\[ v_a = 3 - \left( \frac{K_T}{2} \right) \left[ \left( \frac{W}{L} \right)^2 \left( 2(3 - 0.5) v_a - v_a^2 \right) \right] R_D \]

\[ v_a = 0.1 \]

\[ 0.1 = 3 - \left( \frac{0.06}{2} \right) \left[ (5)(0.1) - (0.1)^2 \right] R_D \]

\[ 0.1 = 3 - 0.0735R_D \]

\[ R_D = 39.5 \text{ K} \]

(b) 

\[ \left( \frac{0.06}{2} \right) (5)(39.5)(v_a - 0.5)^2 + (v_a - 0.5) - 3 = 0 \]

\[ 5.925(v_a - 0.5)^2 + (v_a - 0.5) - 3 = 0 \]

\[ (v_a - 0.5) = V_{oA} = \frac{-12 \sqrt{1 + 4(5.925)(5)}}{2(5.925)} \]

\[ V_{oA} = 0.632 \text{ V} \]

\[ V_a = 1.132 \text{ V} \]

16.6

(a) From Equation (16.23)

\[ K_T \left[ 2(3 - 0.5)(0.25) - (0.25)^2 \right] = (3 - 0.25 - 0.5)^2 \Rightarrow \frac{K_T}{K_I} = 4.26 \]

(b) \[ \frac{K_T}{K_I} \left[ 2(2.5 - 0.5)(0.25) - (0.25)^2 \right] = (3 - 0.25 - 0.5)^2 \Rightarrow \frac{K_T}{K_I} = 5.4 \]

\[ I_D = K_I (V_{GS} - V_{TH}) = K_I (V_{GS} - V_{TH})^2 \]

\[ = \left( \frac{0.08}{2} \right) \left[ (3 - 0.25 - 0.5)^2 \right] = 0.203 \text{ mA} \]

\[ P = I_D \cdot V_{GS} - (0.203)(3) = 0.608 \text{ mW} \]

for both parts (a) and (b).

16.4

HW solution

\[ 0.25 = \sqrt{3} \Rightarrow I = 75.76 \mu \text{A} \]

\[ R = \frac{0.07576}{0.25} \Rightarrow R = 41.6 \text{ K} \]

\[ I = \left( \frac{K_T}{2} \right) \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 \]

\[ 75.76 = \left( \frac{80}{2} \right) \left( \frac{W}{L} \right) \left[ (3 - 0.8)^2 \right] \Rightarrow \left( \frac{W}{L} \right) = 0.303 \]

(b) 

\[ V_{GS} = V_{GS} - V_{TH} \]

\[ I_D = K_I (V_{GS} - V_{TH}) = \frac{V_{GS} - V_{TH}}{R} \]

\[ \left( \frac{0.08}{2} \right) \left( 0.303 \right) \left( (V_{GS} - 1.66_{gs} + 0.64) \right) - \frac{3.3 - (V_{GS} - 0.8)}{41.6} \]

\[ 0.054(5.925 + 0.64) = 4.1 - V_{oA} \]

\[ 0.054V_{gs} + 0.0404_{gs} - 3.777 = 0 \]

\[ V_{oA} = -0.193 \text{ V} \]

\[ V_{gs} = 2.55 \text{ V} \]

For \( 0.8 \leq V_{gs} \leq 2.55 \text{ V} \)

Transistor biased in saturation region

16.9

\[ V_{out} = V_{gs} - V_{oA} = \text{Logic 1} \]

So

(a) \( V_{gs} = 4 \text{ V} \Rightarrow V_{out} = 3 \text{ V} \)

(b) \( V_{gs} = 5 \text{ V} \Rightarrow V_{out} = 4 \text{ V} \)

(c) \( V_{gs} = 6 \text{ V} \Rightarrow V_{out} = 5 \text{ V} \)

(d) \( V_{gs} = 7 \text{ V} \Rightarrow V_{out} = 5 \text{ V} \), since \( V_{oB} = 0 \)

For \( V_I = V_{oA} \)

\[ K_T \left[ 2(V_I - V_T) V_{oA} - V_I^2 \right] = K_I \left[ V_{gs} - V_{oA} - V_T \right]^2 \]

Then

(a) \( \left( \frac{1}{2} \right) \left[ 2(3 - 1)(V_{gs} - V_{oA}) \right] = (0.4) \left[ 4 - V_{oA} - 1 \right] \Rightarrow V_{oA} = 0.657 \text{ V} \)

(b) \( \left( \frac{1}{2} \right) \left[ 2(4 - 1)(V_{gs} - V_{oA}) \right] = (0.4) \left[ 5 - V_{oA} - 1 \right] \Rightarrow V_{oA} = 0.791 \text{ V} \)

(c) \( \left( \frac{1}{2} \right) \left[ 2(5 - 1)(V_{gs} - V_{oA}) \right] = (0.4) \left[ 6 - V_{oA} - 1 \right] \Rightarrow V_{oA} = 0.935 \text{ V} \)
CMOS Inverter Load Lines

\[ I_{DD} = I_{DL} \]

(a) \[ P = I_{DD} \cdot V_{DD} \]
\[ 150 = I_{DD} \cdot 3 \Rightarrow I_{DD} = 50 \mu A \]

(b) \[ I_{DD} = K_{L} \left(V_{DD}^{2} - V_{DD}^{2}\right) \]
\[ 50 = \frac{(0.05)}{2} \left(\frac{V}{\sqrt{L}}\right)^{2} \Rightarrow \left(\frac{V}{\sqrt{L}}\right)^{2} = 1.25 \]

\[ K_{L} = \frac{W}{L} \]
\[ K_{L1} = \frac{W}{L} \]
\[ K_{L} = 2.04 \Rightarrow \left(\frac{W}{L}\right) = 2.55 \]

For the Load:
\[ V_{OL} = V_{DD} + V_{DD} = 3 - 1 \Rightarrow V_{OL} = 2 \]
\[ \sqrt{2.04} (V - 0.5) = \left[\left(-1\right)\right] \Rightarrow V_{OL} = 1.20 \]

For the Driver:
\[ V_{OL} = V_{DD} - V_{DD} = 1.20 - 0.5 \Rightarrow V_{OL} = 0.70 \]
\[ \frac{V}{\sqrt{L}} = 1.20 \]

DC Analysis of the CMOS Inverter

Complete voltage transfer characteristics, CMOS Inverter

0.25um, W/L = 1.5, W/L = 4.5, V_{DD} = 2.5V, V_{SS} = 0.4V, V_{Tn} = -0.4V
The transition point for the NMOS
\[ V_{GNS} = V_{GSN} - V_{TN} \]
from above graph

\[ V_{GSN} = V_{DD} - V_{TP} \]
NMOS input voltage at the transition point

\[ K_d \left( V_{GSN} - V_{TN} \right)^2 = K_d \left( V_{DD} - V_{TP} \right)^2 \]

Transition point loci for PMOS

\[ V_{GSP} = V_{PP} + V_{TP} \]

When both transistors are in saturation
two drain currents equal

\[ K_d \left( V_{GSN} - V_{TN} \right)^2 = K_d \left( V_{DD} - V_{TP} \right)^2 \]
\[ K_s \left( V_{t} - V_{TN} \right)^2 = K_s \left( V_{DD} - V_{TP} \right)^2 \]

\[ V_d = \frac{V_{DD} + V_{TP} + \sqrt{K_d V_{TN} K_p}}{1 + \frac{K_d}{K_s}} \]
input voltage is a constant

\[ K_d \left( V_{GSN} - V_{TN} \right)^2 = K_d \left( V_{DD} - V_{TP} \right)^2 \]

NMOS output voltage at the transition point

\[ V_{OP} = V_{PP} + V_{TP} \]

\[ V_{OP} = V_{PP} + V_{TP} \]

\[ v_{OP} = v_{GSN} + v_{TP} \]

When the input voltage is just greater than \( V_{TN} \)
\[ v_{r} = v_{GSN} = V_{TN} \]
NMOS begins to conduct

\[ v_{DSN} \approx V_{DD} \]
NMOS is biased in the saturation region

\[ v_{DSN} \text{ is small} \]
PMOS is biased in the nonsaturation region.

\[ I_{DN} = I_{DP} \]

\[ K_d \left( V_{GSN} - V_{TN} \right)^2 = K_d \left( V_{DD} - v_{r} + v_{TP} \left( V_{DD} - v_{r} \right) - \left( V_{DD} - V_{TP} \right)^2 \right) \]

\[ v_{r} \text{ and } v_{r} \text{ relationship as long as} \]
NMOS: saturation, PMOS: nonsaturation.
DC Analysis of the CMOS Inverter

Complete voltage transfer characteristics

- **NMOS**: nonsaturation
- **PMOS**: saturation

**Example 16.9**

Objective: Determine the critical voltages on the voltage transfer curve of a CMOS inverter.

Consider a CMOS inverter biased at $V_{DD} = 5\, \text{V}$ with transistor parameters of $K_N = K_P$ and $V_{TN} = -V_{TP} = 1\, \text{V}$. Then consider another CMOS inverter biased at $V_{DD} = 10\, \text{V}$ with the same transistor parameters.

For $V_{DD} = 5\, \text{V}$

- $V_{OL} = 0\, \text{V}$
- $V_{OH} = V_{IP} - V_{TP} = 2.5 - (-1) = 3.5\, \text{V}$
- $V_{ONL} = V_{IN} - V_{TN} = 2.5 - 1 = 1.5\, \text{V}$

For $V_{DD} = 10\, \text{V}$

- $V_{OL} = 10\, \text{V}$
- $V_{OH} = 5\, \text{V}$
- $V_{ONL} = V_{IN} - V_{TN} = 5 - 1 = 4\, \text{V}$

Input voltage at the PMOS and NMOS transition points,

$$v_I = v_B = \frac{V_{DD} + V_{TP} + \sqrt{K_N V_{TN}}}{1 + \sqrt{\frac{K_N}{K_P}}}$$

$$v_B = \frac{5 + (-1) + \sqrt{1}}{1 + \sqrt{1}} = 2.5\, \text{V}$$

Output voltage at the transition point for the PMOS

$$V_{OP} = V_{IP} - V_{TP} \quad V_{OH} = V_{IP} - V_{TP} = 2.5 - (-1) = 3.5\, \text{V}$$

Output voltage at the transition point for the NMOS

$$V_{ONL} = V_{IN} - V_{TN} \quad V_{ON} = V_{IN} - V_{TN} = 2.5 - 1 = 1.5\, \text{V}$$

For $V_{DD} = 10\, \text{V}$

- $V_B = 5\, \text{V}$
- $V_{ONL} = 6\, \text{V}$
- $V_{ON} = 4\, \text{V}$
The transistor $K_N$ is also known as "pull down" device because it is pulling the output voltage down towards ground.

The transistor $K_P$ is known as the "pull up" device because it is pulling the output voltage up towards $V_{DD}$. This property speeds up the operation considerably.

The static power dissipation during both extreme cases (logic 1 or 0) is almost zero because $i_{DP} = i_{DN} = 0$.

CMOS inverter: series combination of PMOS and NMOS

To form the input, gates of the two MOSFET are connected.
To form the output, the drains are connected together.

The transistor $K_N$ is also known as "pull down" device because it is pulling the output voltage down towards ground.

The transistor $K_P$ is known as the "pull up" device because it is pulling the output voltage up towards $V_{DD}$. This property speeds up the operation considerably.

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

DC Analysis of the CMOS Inverter

Ideally, the current in the CMOS inverter in either steady-state condition is zero: quiescent power dissipation is zero.

Due to the reverse-biased pn junctions, the power dissipation may be in the nanowatt range rather than in the milliwatt range of NMOS inverters.

Without this feature, VLSI would not be possible.

DC Analysis of the CMOS Inverter

CMOS Inverter Design Consideration

- The CMOS inverter usually designed to have,
  \[
  V_{TN} = |V_{TP}|
  \]

- $k_N \left( \frac{W}{L} \right) = k_P \left( \frac{W}{L} \right)$ But $k_N > k_P$ (because $\mu_N > \mu_P$)

How equation (2) can be satisfied?

- This can be achieved if width of the PMOS is made two or three times that of the NMOS device.
- This is very important in order to provide a symmetrical transition, results in wide noise margin.
For the CMOS inverter in Figure 16.34, let $V_{TN} = +0.4\, \text{V}$, $V_{TP} = -0.4\, \text{V}$, $k'_p = 80\, \mu\text{A/V}^2$, $k'_n = 40\, \mu\text{A/V}^2$, and $V_{PD} = 3.3\, \text{V}$. (a) Let $(W/L)_p = 2$ and $(W/L)_n = 4$. (i) Find the transition points for the p-channel and n-channel transistors. $V_{It}$, $V_{OP}$, $V_{ON}$.

(ii) Find $v_T$ when $V_{OP} = 0.4\, \text{V}$ and when $V_{OP} = 2.9\, \text{V}$.

(b) For $(W/L)_p = (W/L)_n = 2$, repeat part (a).
Example 16.29

(b) \( K_p = \frac{80}{2} = 40 \mu A/V^2 \)
\( K_n = \frac{40}{2} = 20 \mu A/V^2 \)

\[ K_p = \frac{W}{L} \]

Transition points

PMOS: \( V_{on} = 1.44 - (-0.4) \Rightarrow V_{on} = 1.84 \text{V} \)

NMOS: \( V_{on} = 1.44 - 0.4 \Rightarrow V_{on} = 1.04 \text{V} \)

For \( V_n = 0.4 \text{V} \):
\[ (40)[(33 - V_n - 0.4)(0.4) - (0.4)^2] = \frac{80}{40} \]
\( V_n = 1.62 \text{V} \)

For \( V_n = 2.9 \text{V} \): NMOS Sat. PMOS: Non-sat
\[ (40)[(33 - V_n - 0.4)(0.4) - (0.4)^2] = \frac{80}{40} \]
\( V_n = 1.16 \text{V} \)

Figure 16.34 CMOS inverter

CMOS Inverter \( V_{TC} \)

Effects of \( V_n \) adjustment

- Result from changing \( k_p/k_n \) ratio:
  - Inverter threshold: \( V_n \neq \frac{V_{DD}}{2} \)
  - Rise and fall delays unequal
  - Noise margins not equal

- Reasons for changing inverter threshold:
  - Want a faster delay for one type of transition (rise/fall)
  - Remove noise from input signal: increase one noise margin at expense of the other

Problem 16.31

16.31 Consider the series of CMOS inverters in Figure P16.31. The threshold voltages of the n-channel transistors are \( V_{TN} = 0.8 \text{V} \), and the threshold voltages of the p-channel transistors are \( V_{TP} = -0.8 \text{V} \). The conduction parameters are all equal.

(a) Determine the range of \( V_{IN} \) for which both \( X_1 \) and \( X_2 \) are biased in the saturation region. (b) If \( V_{IN} = 0.6 \text{V} \), determine the values of \( V_{01}, V_{02} \), and \( V_{03} \).

By symmetry, \( V_{IN} = 2.5 \text{V} \)

\( V_{0P1} = 2.5 + 0.8 = 3.3 \text{V} \)
and \( V_{0N1} = 2.5 - 0.8 = 1.7 \text{V} \)

So \( 1.7 \leq m_1 \leq 3.3 \text{V} \)
Problem 16.31

Example 16.31

Consider the series of CMOS inverters in Figure P16.31. The threshold voltages of the n-channel transistors are $V_{TH} = 0.8$ V, and the threshold voltages of the p-channel transistors are $V_{TP} = -0.8$ V. The conduction parameters are all equal.

(a) Determine the range of $V_{GS}$ for which both $N_1$ and $P_1$ are biased in the saturation region.

(b) If $V_{GS} = 0.6$ V, determine the values of $V_{DS}$, $V_{DS}$, and $V_T$.

CMOS inverter currents

- When the output of a CMOS inverter is either at a logic 1 or 0, the current in the circuit is zero.
- When the input voltage is in the range $V_{IN} < V_{TH} < |V_{TP}|$ both transistors are conducting and a current exists in the inverter.
CMOS inverter currents

- When PMOS transistor is biased in the saturation region
  - The current in the inverter is controlled by $v_{SGP}$ and the NMOS $v_{DSN}$ adjusts such that $i_{DP} = i_{DN}$.
  - As long as PMOS transistor is biased in the saturation region, the square root of the inverter current is linear function of the input voltage.

At the inverter switching point, both transistors are biased in the saturation region and both transistors influence the current. The actual current characteristic does not have a sharp discontinuity in the slope.

Power Dissipation

- There is no power dissipation in the CMOS inverter when the output is either at logic 0 or 1. However, during switching of the CMOS inverter from low logic 0 to logic 1, current flows and power is dissipated.
- Usually CMOS inverter and logic circuit are used to drive other MOS devices by connecting a capacitor across the output of a CMOS inverter. This capacitor must be charged and discharged during the switching cycle.
**NMOS Transistor Capacitances**

**Triode Region**
- \( C_{ox} \) = Gate-Channel capacitance per unit area (F/m²)
- \( C_{GC} \) = Total gate channel capacitance
- \( C_{GS} \) = Gate-Source capacitance
- \( C_{GD} \) = Gate-Drain capacitance
- \( C_{GSO} \) and \( C_{GDO} \) = overlap capacitances (F/m)

**Saturation Region**
- Drain is no longer connected to channel.

**Cutoff Region**
- Conducting channel region is completely gone.
- \( C_{GB} \) = Gate-Bulk capacitance
- \( C_{GBW} \) = Gate-Bulk capacitance per unit width.

**Switch Model of Dynamic Behavior**
- Gate response time is determined by the time to charge \( C_L \) through \( R_p \) (discharge \( C_L \) through \( R_n \))
CMOS Inverter Power

- Power has three components
  
  - **Static power**: when input isn’t switching
  
  - **Dynamic capacitive power**: due to charging and discharging of load capacitance
  
  - **Dynamic short-circuit power**: direct current from \( V_{DD} \) to \( G_{nd} \) when both transistors are on

---

**CMOS Inverter Power**

**Static Power Consumption**

- Static current: in CMOS there is no static current as long as \( V_{in} < V_{TN} \) or \( V_{in} > V_{DD} + V_{TP} \)
- Leakage current: determined by “off” transistor
- Influenced by transistor width, supply voltage, transistor threshold voltages

**CMOS Inverter Power**

**Dynamic Capacitive Power and Energy stored in the PMOS**

Case I: When the input is at logic 0
- PMOS is conducting and NMOS is in cutoff mode and the load capacitor must be charged through the PMOS device.

  **Power dissipation** in the PMOS transistor:
  \[
  P = \frac{C_L (V_{DD} - V_O)}{2}
  \]

  The current and output voltages are related by,
  \[
  i_L = C_L \frac{dV_O}{dt}
  \]

  Similarly the **energy dissipation** in the PMOS device
  \[
  E_L = \int E_{C,L} \, dt = C_L (V_{DD} - V_O) \int \frac{dV_O}{2} = C_L \frac{V_{DD} - V_O}{2}
  \]

  \[
  E_{C,L} = \int \frac{1}{2} C_L (V_{DD} - V_O)^2 \, dt
  \]

  \[
  E_{C,L} = \frac{1}{2} C_L (V_{DD} - V_O)^2
  \]

**CMOS Inverter Power**

**Dynamic Capacitive Power and Energy stored in the PMOS**

Case II: when the input is high and output is low:
- During switching all the energy stored in the load capacitor is dissipated in the NMOS device because NMOS is conducting and PMOS is in cutoff mode.

  The energy dissipated in the NMOS inverter;

  \[
  E_{NMOS} = \frac{1}{2} C_L (V_{DD} - V_{O(H)})^2
  \]

  The total energy dissipated during one switching cycle;

  \[
  E_T = E_P + E_L + E_{NMOS} + E_{NMOS} = C_L \frac{V_{DD}^2}{2} + C_L \frac{V_{O(H)}^2}{2}
  \]

This implied that the **power dissipation** in the CMOS inverter is directly proportional to switching frequency and \( V_{DD}^2 \).
CMOS Inverter Power

**Dynamic Capacitive Power**

\[ P_{\text{dyn}} = C_L V_D^2 f \]

- Formula for dynamic power
- Does not (directly) depend on device sizes
- Does not depend on switching delay
- Applies to general CMOS gate in which:
  - Switched capacitances are lumped into \( C_L \)
  - Output swings from GND to \( V_{DD} \)
  - Input signal approximated as step function
  - Gate switches with frequency \( f \)

**Dynamic Short-Circuit Power**

- Short-circuit current flows from \( V_{DD} \) to GND when both transistors are on saturation mode.

**Inverter Power Consumption**

**Total Power Consumption**

\[ P_{\text{tot}} = P_{\text{dyn}} + P_{\text{sc}} + P_{\text{stat}} \]

\[ P_{\text{tot}} = C_L V_D^2 f + V_{DD} I_{\text{max}} \left( \frac{t_r + t_f}{2} \right) f + V_{DD} I_{\text{leak}} \]

\[ P_{\text{tot}} \sim C_L V_D^2 f \]

**Power Reduction**

- **Reducing dynamic capacitive power**
  - Lower the voltage!!
    - Quadratic effect on dynamic power
  - Reduce capacitance!!
    - Short interconnect lengths
    - Drive small gate load (small gates, small fan-out)
  - Reduce frequency!!
    - Lower clock frequency
    - Lower signal activity
Power Reduction

- **Reducing short-circuit current**
  - Fast rise/fall times on input signal
  - Reduce input capacitance
  - Insert small buffers to “clean up” slow input signals before sending to large gate

- **Reducing leakage current**
  - Small transistors (leakage proportional to width)
  - Lower voltage

---

### Chapter 16

**MOSFET Digital Circuits**

**Chapter 16.3.4**

**CMOS Inverter Noise Margin**

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**Concept of Noise Margins**

The noise margin for low input is given by:

$$NM_L = V_{OH} - V_{OL}$$

The noise margin for high input is given by:

$$NM_H = V_{OL} - V_{OH}$$

$$V_{OH}$$ and $$V_{IL}$$ determine the noise margins.

For $$V_{IL} < V_T < V_{OH}$$, the inverter gain is greater than unity, and the output signal changes rapidly with input voltage.

For $$V_T < V_{IL}$$ and $$V_T > V_{OH}$$, the inverter gain is less than unity, and the output changes slowly with input voltage.

The inverter gain is defined as:

$$G = \frac{dV_O}{dV_I}$$

The noise margin is determined by the input voltage swing and the inverter's gain.
CMOS Inverter Noise Margins

The relationship between the input and output voltages of CMOS when CMOS is symmetrical is:

\[ i_{DN} = i_{DP} \]

\[ K_N[V_{GS>N} - V_{TN}]^2 = K_P[2(V_{DDP} + V_{TP})(V_{PP} - V_{DDP} - V_{I})] \]

\[ K_P[V_{GS>N} - V_{TN}]^2 = K_P[2(V_{DDP} - V_{TP})V_{PP} - V_{DDP} - V_{I}] \]

\[ V_I = V_{OL} \left( \frac{K_N}{K_P} \right) = V_{TN} + \frac{1}{2}(V_{DDP} + V_{TP} - V_{TN}) \] for \( K_N = K_P \)

CMOS Inverter Noise Margins

The relationship between the input and output voltages of CMOS when CMOS is non-symmetrical is:

\[ V_0 = V_{OL} \left( \frac{1 + \frac{K_N}{K_P}}{1 + \frac{K_N}{K_P}} \right) V_T + V_{DDP} - \left( \frac{K_N}{K_P} \right) V_{TN} - V_{TP} \]

If CMOS is symmetrical, \( K_N = K_P \)

\[ V_0 = V_{OL} \left( \frac{1 + \frac{K_N}{K_P}}{2} \right) + \left( \frac{K_N}{K_P} \right) \left( V_{DDP} + V_{TP} - V_{TN} \right) \]

\[ K_N[V_I - V_{TN}]^2 = K_P[2(V_{DDP} - V_{I} + V_{TP})(V_{PP} - V_{DDP} - V_{I})] \]

\[ V_I = V_{OL} \left( \frac{K_N}{K_P} \right) = V_{TN} + \frac{1}{2}(V_{DDP} + V_{TP} - V_{TN}) \] for \( K_N = K_P \)

CDMOS Inverter Noise Margins

The relationship between the input and output voltages of CMOS when CMOS is symmetrical is:

\[ K_N[V_I - V_{TN}]^2 = K_P[2(V_{DDP} - V_{I} + V_{TP})(V_{PP} - V_{DDP} - V_{I})] \]

Taking the derivative with respect to \( V_I \):

\[ \frac{dV_0}{dV_I} = -K_N(V_I - V_{TN}) + \frac{K_N}{K_P} [V_{DDP} - V_{I} + V_{TP}] \]

\[ V_0 = V_{OL} \left( \frac{1 + \frac{K_N}{K_P}}{2} \right) + \left( \frac{K_N}{K_P} \right) \left( V_{DDP} + V_{TP} - V_{TN} \right) \]

\[ V_I = V_{OL} \left( \frac{K_N}{K_P} \right) = V_{TN} + \frac{1}{2}(V_{DDP} + V_{TP} - V_{TN}) \] for \( K_N = K_P \)

CDMOS Inverter Noise Margins

The relationship between the input and output voltages of CMOS when CMOS is non-symmetrical is:

\[ K_N[V_I - V_{TN}]^2 = K_P[2(V_{DDP} - V_{I} + V_{TP})(V_{PP} - V_{DDP} - V_{I})] \]

Taking the derivative with respect to \( V_I \):

\[ \frac{dV_0}{dV_I} = -K_N(V_I - V_{TN}) + \frac{K_N}{K_P} [V_{DDP} - V_{I} + V_{TP}] \]

\[ V_0 = V_{OL} \left( \frac{1 + \frac{K_N}{K_P}}{2} \right) + \left( \frac{K_N}{K_P} \right) \left( V_{DDP} + V_{TP} - V_{TN} \right) \]

\[ V_I = V_{OL} \left( \frac{K_N}{K_P} \right) = V_{TN} + \frac{1}{2}(V_{DDP} + V_{TP} - V_{TN}) \] for \( K_N = K_P \)
CMOS Inverter Noise Margins

If CMOS is symmetrical, $K_N = K_P$

$$v_O = V_{OLU} + \gamma (1 + \frac{K_N}{K_P}) - V_{DD} - \left( \frac{K_N}{K_P} \right) V_{TN} - V_{TP}$$

$$K_N [2(\gamma - V_{TX}) V_O - V_O^2] = K_P (V_{DD} - \gamma + V_{TP})^2$$

$$\gamma = V_{IH(K_N=K_P)} = V_{TN} + \frac{2}{3} (V_{DD} + V_{TF} - V_{TX}) \text{ for } K_N = K_P$$

Summary

Noise Margin of a Symmetrical CMOS Inverter

$$NM_L = V_{IL} - V_{OLU} \quad \text{Noise Margin for low input}$$

$$NM_H = V_{OHL} - V_{IH} \quad \text{Noise Margin for high input}$$

Example 16.11

Objective: Determine the noise margins of a CMOS inverter.
Consider a CMOS inverter biased at $V_{DD} = 5$ V. Assume the transistors are matched with $K_N = K_P$ and $V_{TN} = -V_{TP} = 1$ V.

$$v_I = V_{IL(K_N=K_P)} = V_{TN} + \frac{2}{3} (V_{DD} + V_{TF} - V_{TX})$$

$$V_{IL} = V_{TN} + \frac{2}{3} (V_{DD} + V_{TF} - V_{TN}) = 1 + \frac{2}{3} (5 - 1 - 1) = 2.125 \text{ V}$$

$$v_I = V_{IH(K_N=K_P)} = V_{TN} + \frac{2}{3} (V_{DD} + V_{TF} - V_{TN})$$

$$V_{IH} = V_{TN} + \frac{2}{3} (V_{DD} + V_{TF} - V_{TN}) = 1 + \frac{2}{3} (5 - 1 - 1) = 2.875 \text{ V}$$

$$V_{OLU(K_N=K_P)} = \frac{1}{2} [2(\gamma - V_{DD} - V_{TN} - V_{TP})]$$

$$V_{OLU} = \frac{1}{2} [2(\gamma - V_{DD} - V_{TN} - V_{TP})]$$

$$V_{OLH} = \frac{1}{2} [2(V_{IL} + V_{DD} - V_{TN} - V_{TF})]$$

$$V_{OLH} = \frac{1}{2} [2(V_{IH} + V_{DD} - V_{TN} - V_{TF})]$$

Noise margins

$$NM_L = V_{OLU} - V_{IH} = 4.625 - 2.875 = 1.75 \text{ V}$$

$$NM_H = V_{IH} - V_{OLU} = 2.125 - 0.375 = 1.75 \text{ V}$$
CMOS Logic Circuits

- Large scale integrated CMOS logic circuits including watches, calculators, and microprocessors are constructed by using basic CMOS NOR and NAND gates.

Therefore, understanding of these basic gates is very important for the designing of very large scale integrated (VLSI) logic circuits.

CMOS NOR and NAND Gates

CMOS NOR gate can be constructed by using two parallel NMOS devices and two series PMOS transistors.

The output is at logic 1 when all inputs are low.

For all other possible inputs, output is low or at logic 0.

Two-input CMOS NOR logic circuit

CMOS Logic Circuits

CMOS Logic Circuits

CMOS NOR and NAND Gates

- CMOS NAND gate can be constructed by using two parallel PMOS devices and two series NMOS transistors.

The output is at logic 0 when all inputs are high.

For all other possible inputs, output is high or at logic 1.

Two-input CMOS NAND logic circuit

How can we design CMOS NOR symmetrical gate?

To obtain symmetrical switching times for the high-to-low and low-to-high output transitions, the effective conduction (design) parameters of the composite PMOS and composite NMOS device must be equal.

For the CMOS NOR gate, $K_{CN} = K_{CP}$, effective conduction parameter of the transistor NMOS and two series PMOS.

The effective channel width of the parallel NMOS devices is twice the individual width; similarly, the effective channel length of the series PMOS devices is twice the individual length.

$$k'_{n} = \frac{2W}{L} \implies \frac{k'_{p}}{W} = \frac{k'_{p}}{L} \iff \frac{W}{L} \approx \frac{W}{L}$$

In order to get the symmetrical switching properties, the width to length ratio of PMOS transistor must be approximately eight times that of the NMOS device.

For asymmetrical case, switching time is longer!
**CMOS Logic Circuits**

**How can we design CMOS NOR symmetrical gate?**

Voltage transfer characteristics, two-input CMOS NOR logic circuit for various width-to-length ratios

---

**Concept of Effective Width to Length Ratios**

**Parallel combination**

For the NOR gate the effective width of the drivers transistors doubles. The effective aspect ratio is increased.

**Series combination**

For the NAND gate the effective length of the driver transistors doubles. The effective aspect ratio is decreased.

---

**D16.19** In the two-input CMOS NAND gate in Figure 16.45(a), determine the relationship between the \((W/L)_n\) ratios of the n-channel and p-channel transistors such that the composite conduction parameters of the PMOS and NMOS devices are equal. (Ans. \((W/L)_n = 2(W/L)_p\))

**D16.20** Design a three-input CMOS NOR logic gate such that the effective conduction parameters of the composite PMOS and NMOS transistors are equal. Determine \((W/L)_p/(W/L)_n\), where \((W/L)\) is the width-to-length ratio of the individual PMOS and NMOS transistors. (Ans. \((W/L)_p = 18(W/L)_n\))
CMOS Logic Circuits

Fan-In and Fan-Out

- **Fan-in** of a gate is the number of its inputs. Thus a four input NOR gate has a fan-In of 4.
- **Fan-Out** is the maximum number of load gates that may be connected to the output.

Since the CMOS logic gate will be driving other CMOS logic gates, the quiescent current required to drive the other CMOS gates is essentially zero. Thus the maximum fanout is virtually limitless.

However,

- Each additional load gate increases the load capacitance, thereby increasing the charge and discharge time as the driver gate changes state. This places a practical limit on the maximum allowable number of load gates.

Switching Time and Propagation Delay Time

- The dynamic performance of a logic circuit family is characterized by propagation delay of its basic inverter. The propagation delay time is defined as the average of low-to-high propagation delay time and the high-to-low propagation delay time.
- The propagation delay time is directly proportional to the switching time and increases as the fan-out increases. Therefore, the maximum fanout is limited by the maximum acceptable propagation delay time.

- Each additional load gate increases the load capacitance, thereby increasing the charge and discharge time as the driver gate changes state. This places a practical limit on the maximum allowable number of load gates.

Propagation Delay Estimate

- The two modes of capacitive charging/discharging that contribute to propagation delay

![Diagram](image-url)
Switch-level model

Delay estimation using switch-level model (for general RC circuit):

\[ I = C \frac{dV}{dt} \quad \Rightarrow \quad dt = \frac{C}{I} dV \]

\[ I = \frac{V}{R} \quad \Rightarrow \quad dt = \frac{RC}{V} dV \]

\[ t_i - t_i = \int_i^{V} \frac{RC}{V} dV \]

\[ t_p = RC \ln \left( \frac{V_1}{V_0} \right) = \frac{1}{2} \ln \left( \frac{V_{CC}}{V_{CC}} \right) \]

For fall delay \( t_{phl} \), \( V_0 = V_{cc}, \ V_1 = V_{cc}/2 \)

\[ t_p = RC \ln(0.5) \]

\[ t_{phl} = 0.69 R_n C_L \]

\[ t_{plh} = 0.69 R_p C_L \]

Standard RC-delay equations

Chapter 16

MOSFET Digital Circuits

Chapter 16.6

Transmission Gates

- Use of transistors as switches between driving circuits and load circuits are called transmission gates because switches can transmit information from one circuit to another.
- NMOS and CMOS transmission gate.
The bias applied to the transistor determines which terminal acts as the drain and which terminal acts as the source. As an Open Switch

When gate voltage $\phi = 0$, the n-channel transistor is cut-off and the transistor acts as an open switch.

$C_L$, load capacitance: input gate capacitance of a MOS logic circuit. The transistor must be bilateral, must be able to conduct current in either direction. This is a natural feature of MOSFETs.

As an Open Switch

When $\phi = 0$, terminal $a$ acts as the drain since its bias is $V_{DD}$, and terminal $b$ acts as the source since its bias is $V_{SS}$.

Current enters the drain from the input charging up the capacitor. As $CL$ charges up and $V_o$ increases, the gate to source voltage decreases. When the gate to source voltage $VGS$ becomes equal to threshold voltage $VTN$, the capacitance stops charging and current goes to zero.

This implies that output voltage never will be equal to $V_{DD}$, rather it will be lower by $V_{TN}$. This is one of the disadvantages of an NMOS transmission gate when $VI = \text{high}$.

$V_{DD} = V_I$ where $V_I$ is initially (n-channel) zero.

$V_o$ is initially zero.

$V_{DD} - V_I = V_{DD}$.

If $\phi = V_{DD}$, $V_o = V_{DD}$, and $V_o$ is initially (n-channel) zero, terminal $a$ acts as the drain since its bias is $V_{DD}$, and terminal $b$ acts as the source since its bias is zero.

Current enters the drain from the input charging up the capacitor. As $CL$ charges up and $V_o$ increases, the gate to source voltage decreases. When the gate to source voltage $VGS$ becomes equal to threshold voltage $VTN$, the capacitance stops charging and current goes to zero.

This implies that output voltage never will be equal to $V_{DD}$; rather it will be lower by $V_{TN}$. This is one of the disadvantages of an NMOS transmission gate when $VI = \text{high}$.

$V_{DD} = V_I$ where $V_I$ is initially (n-channel) zero.

$V_o$ is initially zero.

$V_{DD} - V_I = V_{DD}$.

If $\phi = V_{DD}$, $V_o = V_{DD}$, and $V_o$ is initially (n-channel) zero, terminal $a$ acts as the drain since its bias is $V_{DD}$, and terminal $b$ acts as the source since its bias is zero.

Current enters the drain from the input charging up the capacitor. As $CL$ charges up and $V_o$ increases, the gate to source voltage decreases. When the gate to source voltage $VGS$ becomes equal to threshold voltage $VTN$, the capacitance stops charging and current goes to zero.

This implies that output voltage never will be equal to $V_{DD}$; rather it will be lower by $V_{TN}$. This is one of the disadvantages of an NMOS transmission gate when $VI = \text{high}$.
Characteristics of NMOS transmission gate (at low input)

- When \( V_{GS} = 0 \) and \( \phi = V_{DD} \)
- and \( V_{DD} = V_{DD} - V_{TN} \) at \( t=0 \) (initially).

It is to be noted that in the present case terminal \( a \) acts as the drain and terminal \( b \) acts as the source.

Under these conditions the gate to source voltage is,

\[
V_{GS} = \phi - V_{I} = V_{DD} - 0 = V_{DD}
\]

This implies that value of \( V_{GS} \) is constant.

In this case the capacitor is fully discharged to zero as the drain current goes to zero.

\[ V_{O} = 0 \]

This implies that the NMOS transistor provide a "good" logic 0 when \( V_{I} \) is low.

 NMOS Transmission Gate

Why NMOS transmission gate does not remain in a static condition?

The reverse leakage current due to reverse bias between terminal \( b \) and ground begins to discharge the capacitor, and the circuit does not remain in a static condition.

NMOS Transmission Gate

As an Open Switch

When \( \phi = V_{DD} \), \( V_{I} = 0 \), and \( V_{DD} = V_{DD} - V_{TN} \) at \( t=0 \),

- terminal \( a \) acts as the source since its bias is zero.
- terminal \( b \) acts as the drain since its bias is high.

Capacitor discharges as current enters the drain. Stop discharging drain current goes zero.

\[ V_{GS} = \phi - V_{I} = V_{DD} - 0 = V_{DD} \]

In this case the capacitor is fully discharged to zero as the drain current goes to zero.

\[ V_{O} = 0 \]

This implies that the NMOS transistor provide a "good" logic 0 when \( V_{I} \) is low.

Example 16.13

Objective: Estimate the rate at which the output voltage \( V_{O} \) in Figure 16.57 decreases with time.

Assume the capacitor is initially charged to \( V_{O} = 4 \) V. Let \( C_{L} = 1 \) pF and assume the reverse-biased p/n junction leakage current is a constant at \( i_{L} = 1 \) nA.

The voltage across the capacitor

\[
v_{O} = \frac{1}{C_{L}} \int_{t}^{t+\Delta t} i_{L} dt + K_{1}
\]

The voltage across the capacitor

\[
v_{O} = 4 - \frac{i_{L}}{C_{L}} t
\]

The initial condition

\[
v_{O}(t = 0) = 4 \text{ V initial condition}
\]

The rate at which the output voltage decreases

\[
\frac{dv_{O}}{dt} = -\frac{i_{L}}{C_{L}} = -\frac{10^{-9}}{10^{-12}} = -1000 \text{ V/s} \Rightarrow -1 \text{ V/ms}
\]

the capacitor would completely discharge in 4 ms.
Example 16.54: Determine the output of an NMOS inverter driven by a source of NMOS transmission gate.

Consider the circuit shown in Figure 16.16. The NMOS inverter is driven by three NMOS transmission gates in series to ensure the threshold voltage of the inverter remains constant. The drain current at the inverter input is equal to zero, and the drain current of the NMOS transmission gates is described below.

(a) Determine the output of the gate when the input voltage is applied to the threshold voltage of the gate.

\( V_{DD} - V_{TN} \)

(b) Determine the output of the gate when the input voltage is applied to the threshold voltage of the gate.

\( V_{DD} - V_{TN} \)

Example 16.52:

**Test Your Understanding**

16.26 The threshold voltage of the NMOS transmission gate transistor in Figure 16.16(a) is \( V_{TH} = 1 \) V. Determine the quiescent output voltage \( V_{DQ} \): (a) \( V_{DQ} = 5 \) V; (b) \( V_{DQ} = 3 \) V, \( \phi = 5 \) V; (c) \( V_{DQ} = 4.2 \) V, \( \phi = 5 \) V; and (d) \( V_{DQ} = 5 \) V, \( \phi = 3 \) V. (Ans. (a) \( V_{DQ} = 4 \) V (b) \( V_{DQ} = 3 \) V (c) \( V_{DQ} = 4 \) V (d) \( V_{DQ} = 2 \) V)

Example 16.52:

**D16.52** For the circuit in Figure 16.52, (a) the input voltage \( v_{I} \) is either 0.1 V or 5 V. Let \( \phi = 5 \) V. The threshold voltages are \( V_{TH} = 1.5 \) V for \( M_{4} \) and \( V_{TH} = 0.8 \) V for all other transistors. The width-to-length ratios are 1 for \( M_{2} \) and \( M_{4} \) and 10 for \( M_{4} \) and \( M_{5} \). (a) What are the logic values of \( v_{D1} \) and \( v_{D2} \)? (b) Design the width-to-length ratios of \( M_{1} \) and \( M_{2} \) such that the logic 0 values of \( v_{D1} \) and \( v_{D2} \) are 0.1 V. (Use the body effect.)

- (a) \( v_{D1}(\text{logic } 1) = 4.2 \text{ V}, v_{D2}(\text{logic } 1) = 5 \text{ V} \)
A CMOS transmission gate can be constructed by parallel combination of NMOS and PMOS transistors, with complementary gate signals.  

The main advantage of the CMOS transmission gate compared to NMOS transmission gate is to allow the input signal to be transmitted to the output without the threshold voltage attenuation.

Example 16.52  

$V_I = 5\ V \Rightarrow V_{G21} = 4.2\ V$

$m_1$ in non-saturation and $m_3$ in saturation.

NMOS Inverter with Enhancement Load

$\frac{W}{L} \cdot \left[ 2(V_{G(a)} - V_{TH})V_0 - V_0^2 \right] = \frac{W}{L} \cdot \left[ (V_{TH} - V_0)^2 \right]$, where $V_0 = 0.67\ V$.

$m_2$ in non-saturation and $m_4$ in saturation.

NMOS Inverter with Depletion Load

$\frac{W}{L} \cdot \left[ 2(V_{G(a)} - V_{TH})V_0 - V_0^2 \right] = \frac{W}{L} \cdot \left[ (V_{TH} - V_0)^2 \right]$, where $V_0 = 2.25\ V$.

$\frac{W}{L} \cdot \left[ 2(V_{G(a)} - V_{TH})V_0 - V_0^2 \right] = \frac{W}{L} \cdot \left[ (V_{TH} - V_0)^2 \right]$, where $V_0 = 3.36\ V$.

Case I: Input High condition

If $\phi = V_{DD}$, $\bar{\phi} = 0$, $V_I = V_{DD}$, and $V_0$ is initially zero,

NMOS terminal $a$ acts as the drain
PMOS terminal $b$ acts as the source

In order to charge the load capacitor, current enters the NMOS drain and the PMOS source.

NMOS: $V_{GNN} = \phi - V_0 = V_{DD} - V_0$

PMOS: $V_{GSP} = \phi - \bar{\phi} = V_{DD} - 0 = V_{DD}$

When $V_0 = V_{DD} - V_{TH}$, the NMOS cuts off and $i_{DS} = 0$ since $V_{GNN} = V_{TH}$.

PMOS continues to conduct since $V_{GSP} = V_{DD}$.

In PMOS, $I_{in} = 0$, when $V_{SHE} = 0$, which would be possible only, if, $V_{in} = V_{DD} - V_{TH}$.

logic ‘1’ is unattenuated

Case II: Input Low condition

If $\phi = V_{DD}$, $\bar{\phi} = 0$, $V_I = 0$, and $V_0 = V_{DD}$ initially,

NMOS terminal $a$ acts as the source
PMOS terminal $b$ acts as the drain

In order to discharge the load capacitor, current enters the NMOS drain and the PMOS source.

NMOS: $V_{GNN} = \phi - \bar{\phi} = V_{DD} - 0 = V_{DD}$

PMOS: $V_{GSP} = V_0 - \bar{\phi} = V_0 - 0 = V_0$

When $V_{SHE} = V_0 = |V_{TH}|$, the PMOS device cuts off and $i_{DP}$ goes to zero. However, since $V_{GNN} = V_{DD}$, the NMOS transistor continues conducting and capacitor $C_L$ completely discharges to zero.

Finally, $V_0 = 0$, which is a good logic 0. $V_{SHE} = V_0 - \bar{\phi} = V_0 - 0 = V_0$.
**CMOS Transmission Gate**

**CMOS Transmission Gate remains in a dynamic condition.**

- If \( V_O = V_{DD} \) and \( \phi = 0 \), then NMOS substrate to terminal ‘b’ pn junction is reverse biased and capacitor \( C_L \) can discharge.
- If \( V_O = 0 \), then the PMOS terminal c-to-substrate pn junction is reverse biased and capacitance \( C_L \) can be charge to a positive voltage.
- This implies that the output high or low of CMOS transmission gate circuit do not remain constant with time (dynamic behavior).

**Test your understanding**

**16.29** Consider the CMOS transmission gate in Figure 16.64(a). Assume transistor parameters of \( V_{TN} = +0.8 \text{ V} \) and \( V_{TP} = -1.2 \text{ V} \). When \( \phi = 5 \text{ V} \), input \( v_i \) varies with time as \( v_i = 0.5t \text{ V} \) for \( 0 \leq t \leq 10 \text{ s} \). Let \( v_o(t = 0) = 0 \) and assume \( C_L = 1 \text{ pF} \). Determine the range of times that the NMOS and PMOS devices are conducting or cut off.

**Exercise 16.29 (a)**

Given that \( V_{TN}=0.8 \text{ V}, V_{TP}=-1.2 \text{ V} \). When \( \phi = 5 \text{ V} \), input \( v_i \) varies with time as \( v_i = 0.5t \text{ V} \) for \( 0 \leq t \leq 10 \text{ s} \). Let \( V_O = 0 \) and \( C_L = 1 \text{ pF} \). Determine the range of the times that the NMOS and PMOS devices are conducting or cutoff.

- NMOS conducting for \( 0 \leq v_i \leq 4.2 \text{ V} \)
- NMOS conducting for \( 0 \leq t \leq 8.4 \text{ s} \)
- NMOS cutoff for \( 8.4 \leq t \leq 10 \text{ s} \)
HW solution

EX16.8
(a) \[ V_T = \frac{V_{DD}}{2} = \frac{2.1}{2} = 1.05 \text{ V} \]
\[ V_{ON} = V_T - V_{PD} = 1.05 - (-0.4) = 1.45 \text{ V} \]
\[ V_{OFF} = V_T - V_{PD} = 1.05 - 0.4 = 0.65 \text{ V} \]

(b) \[ V_T = \frac{2.1 + (-0.4) + \sqrt{0.5(0.4)}}{1 + \sqrt{0.5}} = 1.16 \text{ V} \]
\[ V_{ON} = 1.16 + 0.4 = 1.56 \text{ V} \]
\[ V_{OFF} = 1.16 - 0.4 = 0.76 \text{ V} \]

(c) \[ V_T = \frac{2.1 + (-0.4) + \sqrt{2}(0.4)}{1 + \sqrt{2}} = 0.938 \text{ V} \]
\[ V_{ON} = 0.938 + 0.4 = 1.338 \text{ V} \]
\[ V_{OFF} = 0.538 \text{ V} \]

TYU163
\[ P = i_D \cdot V_{PD} \quad \Rightarrow \quad i_D = \frac{800}{5} = 160 \mu \text{A} \]
\[ i_D = 160 = \frac{35}{2} \left( \frac{W}{L} \right) \left( 1.4 \right)^2 \Rightarrow \left( \frac{W}{L} \right) = 4.66 \]
\[ i_D = 160 \mu \text{A} = \frac{35}{2} \left( \frac{1}{3} \right) \left( \frac{W}{L} \right) \left[ 2(5 - 0.8)(0.12) - (0.12)^2 \right] \Rightarrow \left( \frac{W}{L} \right) = 27.6 \]

TYU164
a. From the load transistor:
\[ i_{ON} = \left( \frac{1}{2} \right) \left( \frac{W}{L} \right) \left( V_{ON} - V_{PD} \right) = \frac{35}{2}(0.5)(5 - 0.15 - 0.7) \]

or
\[ i_{ON} = 150.7 \mu \text{A} \]

Maximum \( V_T \) occurs when either \( A \) or \( B \) is high and \( C \) is high. For the two NMOS is series, the effective¥
\[ k_{OC} \text{ is cut in half, so} \]
\[ i_{ON} = \left( \frac{1}{2} \right) \left( \frac{W}{L} \right) \left( V_{ON} - V_{PD} \right) \left[ 2(V_{ON} - V_{PD})V_{ON} - V_{PD}^2 \right] \]

or
\[ 150.7 = \left( \frac{1}{2} \right) \left( \frac{W}{L} \right) \left[ 2(5 - 0.7)(0.15) - (0.15)^2 \right] \]

which yields
\[ \left( \frac{W}{L} \right) = 13.6 \]

b. \[ P = i_D \cdot V_{PD} = (150.7)(0.5) \Rightarrow P = 75.3 \mu \text{W} \]

16.36
a. \[ V_{ON} \leq V_T \leq V_{ON} \]

By symmetry, \( V_T = 2.5 \text{ V} \)
\[ V_{PD} = 2.5 + 0.8 = 3.3 \text{ V} \]

and \( V_{ON} = 2.5 - 0.8 = 1.7 \text{ V} \)

So \( 1.7 \leq V_T \leq 3.3 \text{ V} \)

b. For \( V_{PD} = 0.6 < V_T \Rightarrow V_{ON} = 5 \text{ V} \)

\( N_1 \) in non-saturation and \( P_2 \) in saturation. From Equation (16.57),
\[ 2(3)(-0.8)(0.6) - (0.6)^2 \]

\( 1.2V_T - 1.32 = 17.64 - 8.4V_T + V_T^2 \)

or
\[ V_T^2 - 9.6V_T + 18.96 = 0 \]

So \( V_T = 2.78 \text{ V} \)

For \( V_{PD} = 0.6 \), both \( N_1 \) and \( P_2 \) in saturation. Then
\[ V_T = 2.5 \text{ V} \]
Chapter 16

Sequential Logic Circuit

Chapter 16.7

MOSFET Digital Circuits

SEQUENTIAL LOGIC CIRCUITS

In the logic circuits that we have considered in the previous sections, such as NOR and NAND logic gates, the output is determined only by the instantaneous values of the input signals. These circuits are therefore classified as combinational logic circuits.

Another class of circuits is called sequential logic circuits. The output depends not only on the inputs, but also on the previous history of its inputs.

This feature gives sequential circuits the property of memory. Shift registers and flip-flops are typical examples of such circuits. We will also briefly consider a full-adder circuit. The characteristic of these circuits is that they store information for a short time until the information is transferred to another part of the system.

The logic circuits considered thus far are called combinational logic circuits. Their output depend only on the present value of input. This implies that these circuit do not have memory.

Another class of the logic circuit that incorporate memory are called sequential logic circuits; that is, their output depend not only the present value of the input, but also on the previous history of inputs. Shift registers and flip-flops are typical examples of such circuits.
**SEQUENTIAL LOGIC CIRCUITS**

**NMOS Dynamic Shift Registers**

- A shift register can be constructed by the combination of transmission gates and inverters.
- If $V_I = V_{DD}$ and $\phi_1 = V_{DD}$, then a logic 1 at $V_{O1}$ would exist at $V_{O2}$.
- The $C_1$ charges through $M_{N1}$. As $V_{O1}$ goes high, $V_{O2}$ goes low. If $\phi_2$ is high, low will be transmitted through $M_{N2}$ and $V_{O4}$ would be at logic 1. Thus logic 1 is shifted from input to output.

In shift register the input signal is transmitted, or shifted, from the input to the output during one clock cycle.

**Dynamic Shift Registers at Various Time**

- Suppose $V_{DD}=5V$ and $V_{TN}=1V$.
- At $t=t_1$, $V_{O1}=5V$, $V_{O2}$ goes low.
- At this time $M_{N2}$ is still in cutoff $(\phi_2=0)$ even though input of $M_{N2}$ has been changed. This implies that $V_{O3}$ and $V_{O4}$ depend on the previous history.
- Similarly at $t=t_2$, $\phi_2$ is high, and logic 0 at $V_{O2}$ is transmitted to $V_{O3}$, which forces $V_{O4}$ to 5V. Thus the input information is transmitted to output during one clock cycle.

NMOS shift register is also dynamic (why?)

- The output charged capacitor does not remain constant with time because it is discharged through the transmission gate transistor.
- In order to prevent logic errors, the clock signal period $T$ must be small compared to effective RC discharge time constant.

For example at $t=t_2$, $V_{O2}=4V$, $\phi_2=0$ and $M_{N2}$ is cutoff. $V_{O3}$ will start to decay and $V_{O2}$ will begin to increase.
CMOS Dynamic Shift Registers

- The operation of the CMOS shift register is similar to the NMOS register except for the voltage levels.
- For example, when \( v_1 = \phi_1 = V_{DD} \), then \( v_{O1} = V_{DD} \) and \( v_{O2} = 0 \) when \( \phi_2 \) goes high, then \( v_{O3} \) switch to zero, \( v_{O4} = V_{DD} \).
- Thus input signal is shifted to the output during one clock cycle.

NMOS R-S Flip Flop

- Flip-flops are bistable circuits usually formed by cross-coupling two NOR gates. The output of the two NOR circuits are connected back to the inputs of the opposite NOR gates.
- When \( S = \text{logic 1} \) and \( R = \text{logic 0} \), then \( Q = \text{logic 1} = V_{DD} \).
- Transistor \( M_2 \) is then also biased in conducting state.
- If \( S \) returns to logic 0, nothing in the circuit can force a change and flip flop stores the previous logic states, although \( M_1 \) turned off (but \( M_2 \) remains tuned on).

NMOS R-S Flip Flop (cont.)

- When \( R = \text{logic 1} \) and \( S = \text{logic 0} \), then \( M_4 \) turn on so output goes low. With \( S = Q = \text{logic 0} \), both \( M_1 \) and \( M_2 \) are cut off and goes high. The flip-flop is now in reset state.
- If both \( S \) and \( R \) inputs go high. Then both outputs \( Q \) and \( \bar{Q} \) would go low, which implies that output is not complementary. This condition is forbidden or nonallowed condition.

CMOS R-S Flip-Flop

- The operation sequence of CMOS R-S flip flop is same as NMOS.
- For example: If \( S = \text{logic 1} \) and \( R = \text{logic 0} \), then \( M_{N1} \), is turned on, \( M_{P1} \), is cut off, and \( Q \) goes low.
- With \( Q = \text{logic 0} \), then both \( M_{N2} \) and \( M_{P4} \) are cut off, both \( M_{P2} \) and \( M_{N4} \) are biased in a conducting state so that the output \( Q \) goes high.
- With \( Q = \text{logic 1} \), \( M_{N4} \) is biased on, \( M_{P4} \) is biased off, and the flip-flop is in a set condition.
- When \( S \) goes low, \( M_{N1} \), turns off, but \( M_{P1} \), remains conducting, so the state of the flip-flop does not change.
CMOS R-S Flip-Flop (cont.)

- When $S =$ logic 0 and $R =$ logic 1, then output $Q$ is forced low, output $\overline{Q}$ goes high, and the flip-flop is in a reset condition.
- Again, a logic 1 at both $S$ and $R$ is considered to be a forbidden or a nonallowed condition, since the resulting outputs are not complementary.

![CMOS R-S Flip-Flop](image)

Static vs Dynamic Storage

- **Static storage**
  - preserve state as long as the power is on
  - have positive feedback (regeneration) with an internal connection between the output and the input
  - useful when updates are infrequent (clock gating)

- **Dynamic storage**
  - store state on parasitic capacitors
  - only hold state for short periods of time (milliseconds)
  - require periodic refresh
  - usually simpler, so higher speed and lower power

Static D-type Flip-Flop

- A D-type flip-flop is used to provide a delay. The logic bit on the D input is transferred to the output at the next clock pulse.

When the CMOS transmission gate turn off ($\phi=0$), the pn junction in the $M_{P2}$ transmission gate transistor is reverse biased.

![CMOS D-type Flip-Flop](image)