Chapter 16

MOSFET Digital Circuits

Chapter 16.1

NMOS Inverter

MOSFET Digital Circuits

- In the late 70s as the era of LSI and VLSI began, NMOS became the fabrication technology of choice.
- Later the design flexibility and other advantages of the CMOS were realized, CMOS technology then replaced NMOS at all level of integration.
- The small transistor size and low power dissipation of CMOS circuits, demonstration principal advantages of CMOS over NMOS circuits.

NMOS Inverter

- For any IC technology used in digital circuit design, the basic circuit element is the logic inverter.
- Once the operation and characterization of an inverter circuits are thoroughly understood, the results can be extended to the design of the logic gates and other more complex circuits.

MOSFET Digital Circuits

NMOS logic circuits

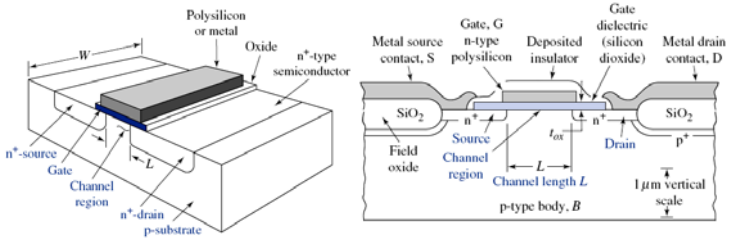
CMOS logic circuits
complementary MOS

NMOS INVERTERS
MOS inverter

NOR and NAND gates

The inverter is the basic circuit of most MOS logic circuits.

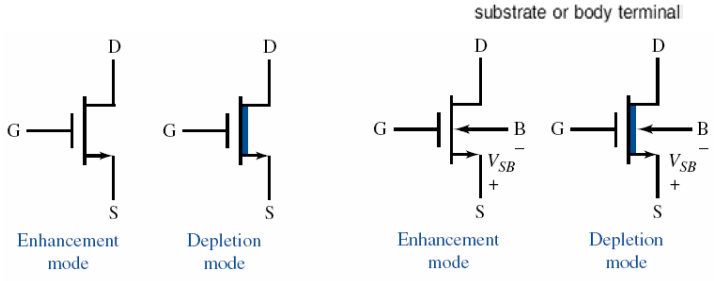
n-channel MOSFET



n-channel MOSFET

the channel length is the same for all transistors, while the channel width is variable.

n-channel MOSFET



n-channel MOSFET

Chap.3 *n*-Channel MOSFET Formulas

- **Transition points**

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

V_{TN} n-channel threshold voltage

- **Saturation region** $v_{DS} > v_{DS}(\text{sat})$ $v_{GS} > V_{TN}$

$$i_D = K_n(v_{GS} - V_{TN})^2$$

- **Nonsaturation region** $v_{DS} < v_{DS}(\text{sat})$

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$$

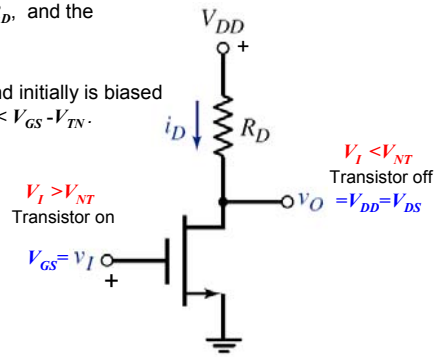
$K_n = \frac{W\mu_n C_{ox}}{2L}$ conduction parameter

NMOS Inverter

- For any IC technology used in digital circuit design, the basic circuit element is the logic inverter.
- Once the operation and characterization of an inverter circuits are thoroughly understood, the results can be extended to the design of the logic gates and other more complex circuits.

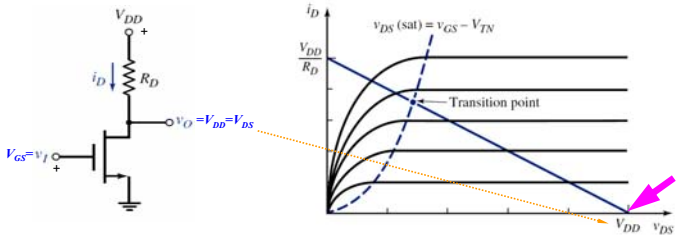
NMOS Inverter

- If $V_I < V_{TN}$, the transistor is in **cutoff** and $i_D = 0$, there is no voltage drop across R_D, and the output voltage is $V_o = V_{DD} = V_{DS}$
- If $V_I > V_{TN}$, the transistor is **on** and initially is biased in **saturation region**, since $V_{DS} < V_{GS} - V_{TN}$.



- As the input voltage increases (V_{GS}), the drain to source voltage (V_{DS}) decreases and the transistor inter into the **nonsaturation region.**

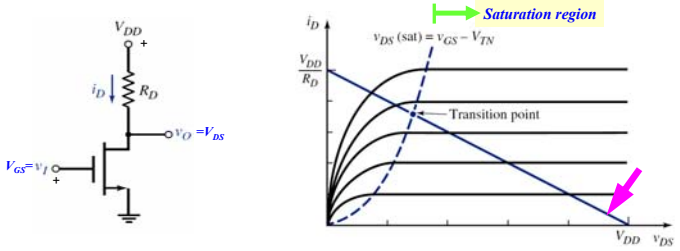
NMOS Inverter with Resister Load



Cut-off

- If $V_I < V_{TN}$, the transistor is in **cutoff** and $i_D = 0$, there is no voltage drop across R_D, and the output voltage is $V_o = V_{DD} = V_{DS}$

NMOS Inverter with Resister Load



Saturation Region

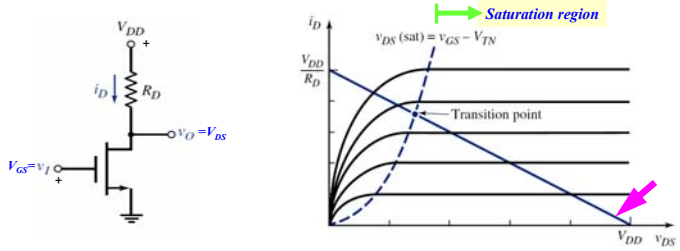
- As the **input** is increased slightly above the V_{TN}, the transistor turns on and is in the **saturation region**.

$$v_O = V_{DD} - i_D R_D$$

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_I - V_{TN})^2$$

$$\boxed{v_O = V_{DD} - K_n R_D (v_I - V_{TN})^2}$$

NMOS Inverter with Resister Load



Transition Region

- As the **input** voltage is further increases and voltage drop across the R_D become sufficient to reduce the V_{DS} such that $V_{DS} \le V_{GS} - V_{TN}$ $\quad v_{DS}(\text{sat}) = v_{GS} - V_{TN}$
- The Q-point of the transistor moves up the load line.

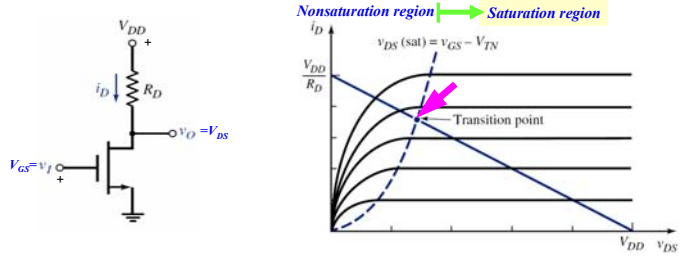
$$v_O = V_{DD} - K_n R_D (v_I - V_{TN})^2$$

At the transition point, $V_{Ot} = V_{It} - V_{TN}$

V_{Ot} drain-to-source voltage
V_{It} gate-to-source voltage

$$K_n R_D (V_{It} - V_{TN})^2 + (V_{It} - V_{TN}) - V_{DD} = 0$$

NMOS Inverter with Resister Load



Nonsaturation Region

- As the **input** voltage becomes greater than V_{It}, the Q-point continues to move up the load line, and the transistor becomes biased in the nonsaturation region.

$$i_D = K_n\left[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2\right] = K_n\left[2(v_I - v_{TN})v_O - v_O^2\right]$$

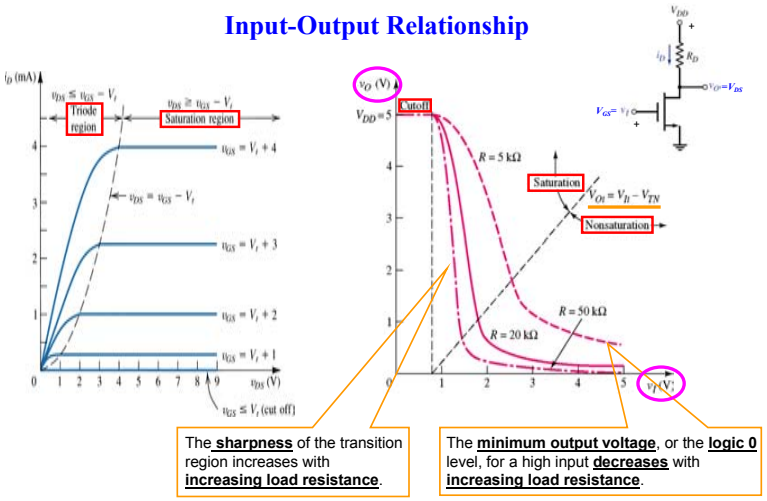
($v_{GS} = v_I$, $v_{DS} = v_O$)

$$v_O = V_{DD} - i_D R_D$$

$$v_O = V_{DD} - K_n R_D\left[2(v_I - V_{TN})v_O - v_O^2\right]$$

NMOS Inverter with Resister Load

Input-Output Relationship



The **sharpness** of the transition region increases with **increasing load resistance**.

The **minimum output voltage**, or the **logic 0** level, for a high input **decreases** with **increasing load resistance**.

Summary of NMOS inverter with Resister Load

Current-Voltage Relationship

Saturation Region

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_I - V_{TN})^2$$

$$v_O = V_{DD} - K_n R_D(v_I - V_{TN})^2$$

Transition Region

$$V_{Ot} = V_{It} - V_{TN}$$

$$K_n R_D(V_{It} - V_{TN})^2 + (V_{It} - V_{TN}) - V_{DD} = 0$$

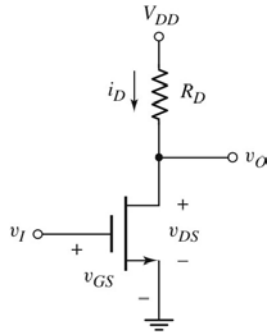
Nonsaturation Region

$$i_D = K_n\left[2(v_I - v_{TN})v_O - v_O^2\right]$$

$$v_O = V_{DD} - K_n R_D\left[2(v_I - V_{TN})v_O - v_O^2\right]$$

Example

For the NMOS inverter shown in Fig. $V_{DD} = 3$V. Assume transistor parameters of $K'_n = 60\ \mu A/v^2$, W/L = 5, and $V_{TN} = 0.5$ V. (a) Find the value of R_D such that $v_o = 0.1$ V when $v_I = 3$ V. (b) Using the results of part (a) determine the transition point for the driver transistor



EX16.2

(a)

$v_o = V_{DD} - I_D R_D$

$v_o = 3 - \left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)\left[2(3-0.5)v_o - v_o^2\right]R_D$

$v_o = 0.1$

$0.1 = 3 - \left(\frac{0.06}{2}\right)(5)\left[(5)(0.1) - (0.1)^2\right]R_D$

$0.1 = 3 - 0.0735 R_D$

$R_D = 39.5\ \text{K}$

(b)

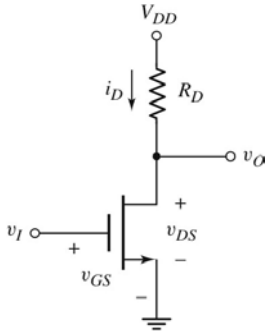
$\left(\frac{0.06}{2}\right)(5)(39.5)(V_{It} - 0.5)^2 + (V_{It} - 0.5) - 3 = 0$

$5.925(V_{It} - 0.5)^2 + (V_{It} - 0.5) - 3 = 0$

$(V_{It} - 0.5) = V_{Ot} = \frac{-1 \pm \sqrt{1 + 4(5.925)(3)}}{2(5.925)}$

$V_{Ot} = 0.632\ \text{V}$

$V_{It} = 1.132\ \text{V}$



n-Channel MOSFET connected as saturated load device

- An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter.
- Since the gate and drain of the transistor are connected, we have $V_{GS}=V_{DS}$

When $V_{GS}=V_{DS}>V_{TN}$ *a non zero drain current is induced in the transistor and thus the transistor operates in saturation only. And following condition is satisfied.*

$V_{DS}>(V_{GS}-V_{TN})$

$V_{DS}\ (sat)= (V_{DS}-V_{TN})$ *because* $V_{GS}=V_{DS}$ *or* $V_{DS}\ (sat)= (V_{GS}-V_{TN})$

In the saturation region the drain current is $i_D=K_n(V_{GS}-V_{TN})^2 = K_n(V_{DS}-V_{TN})^2$

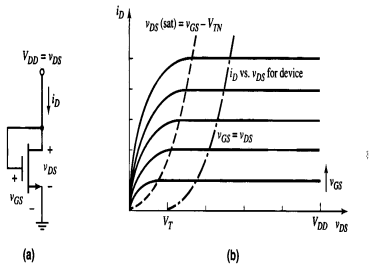
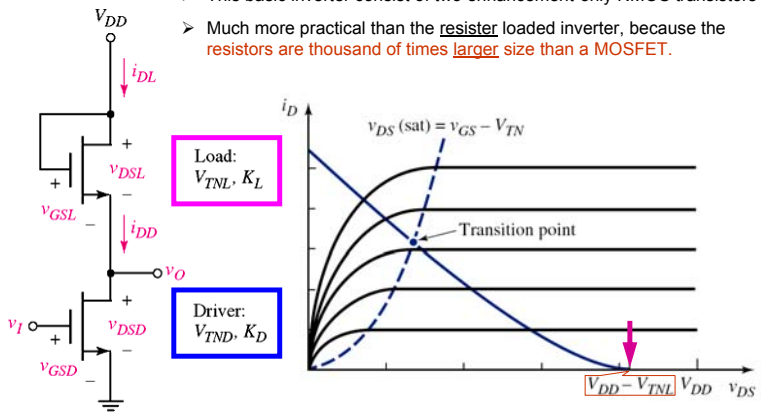


Figure 16.7 (a) n-channel MOSFET connected as saturated load device and (b) current–voltage characteristics of saturated load device

The i_D versus v_{DS} characteristics are shown in Figure 16.7(b), which indicates that this device acts as a nonlinear resistor.

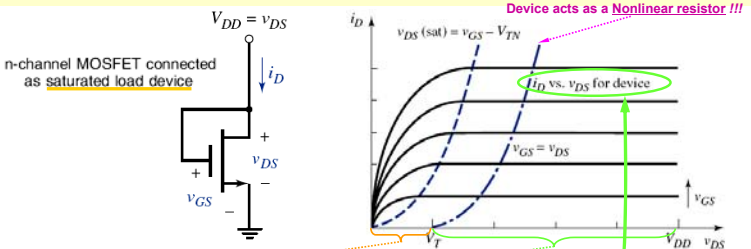
NMOS Inverter with Enhancement Load

- This basic inverter consist of two enhancement-only NMOS transistors
- Much more practical than the resister loaded inverter, because the resistors are thousand of times larger size than a MOSFET.



NMOS Inverter with Enhancement Load

- An n-channel **enhancement-mode MOSFET** with gate connected to the drain can be used as a **load device**.



For $v_{GS} = v_{DS} \le V_{TN}$, the drain current is zero.

$v_{GS} = v_{DS} > V_{TN}$, a nonzero drain current is induced in the device.

$v_{DS} > (v_{GS} - V_{TN}) = (v_{DS} - V_{TN}) = v_{DS}(\text{sat})$

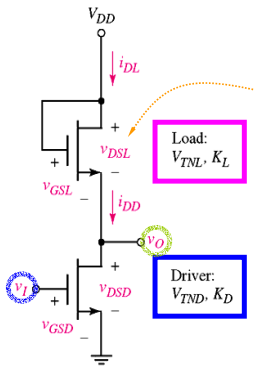
$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2$ — Nonlinear resistor !!!

A transistor with this connection always operates in the saturation region when not in cutoff.

NMOS Inverter with Enhancement Load

When $v_I < V_{TND}$ driver is cut off and the drain currents are zero.

$$i_{DL} = 0 = K_L(v_{DSL} - V_{TNL})^2$$



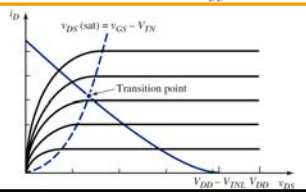
$$v_{DSL} = V_{DD} - v_O$$

$$\rightarrow v_{DSL} - V_{TNL} = V_{DD} - v_O - V_{TNL} = 0$$

maximum output voltage

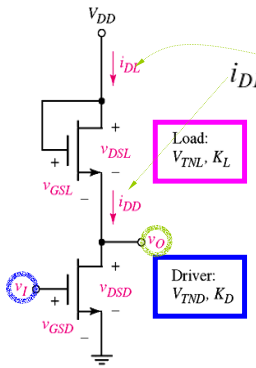
$$v_{O,\max} \equiv V_{OH} = V_{DD} - V_{TNL}$$

For the enhancement-load NMOS inverter, the maximum output voltage, which is the logic 1 level, does not reach the full V_{DD} value.



NMOS Inverter with Enhancement Load

When v_I (just greater than) V_{TND} driver transistor turns on and is biased in the saturation region.



$$i_{DD} = i_{DL}$$

two drain currents are equal since the output will be connected to the gates of other MOS transistors.

$$K_D(v_{GSD} - V_{TND})^2 = K_L(v_{GSL} - V_{TNL})^2$$

$$K_D(v_I - V_{TND})^2 = K_L(V_{DD} - v_O - V_{TNL})^2$$

$$v_O = V_{DD} - V_{TNL} - \sqrt{\frac{K_D}{K_L}}(v_I - V_{TND})$$

As the input voltage increases, the driver Q-point moves up the load curve and the output voltage decreases linearly with v_I.

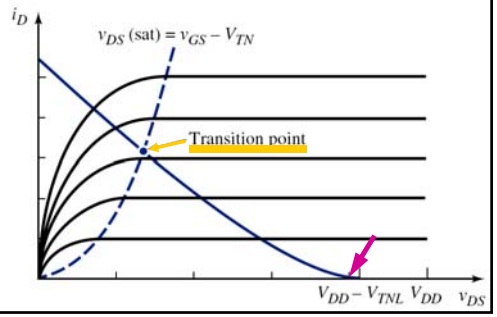
NMOS Inverter with Enhancement Load

At the driver transition point,

$$v_{DSD}(\text{sat}) = v_{GSD} - V_{TND} \quad \text{or} \quad V_{OI} = V_{It} - V_{TND}$$

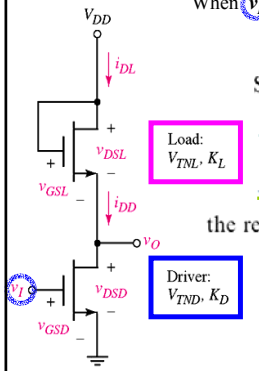
$$v_O = V_{DD} - V_{TNL} - \sqrt{\frac{K_D}{K_L}}(v_I - V_{TND})$$

$$V_{It} = \frac{V_{DD} - V_{TNL} + V_{TND}\left(1 + \sqrt{\frac{K_D}{K_L}}\right)}{1 + \sqrt{\frac{K_D}{K_L}}}$$



NMOS Inverter with Enhancement Load

When $v_I > V_{It}$ the driver transistor Q-point continues to move up the load curve and the driver becomes biased in the nonsaturation region.



Since $i_{DD} = i_{DL}$,

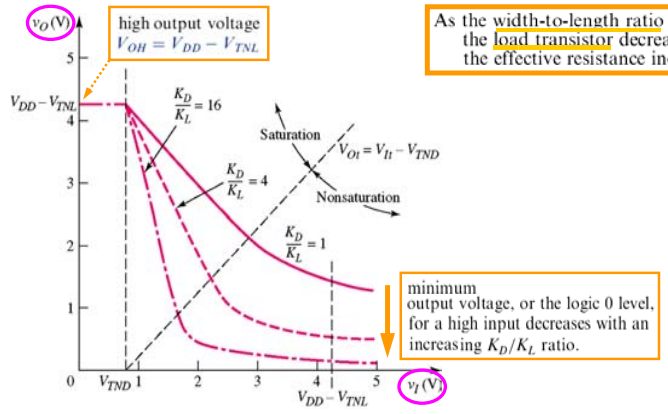
$$K_D[2(v_{GSD} - V_{TND})v_{DSD} - v_{DSD}^2] = K_L(v_{DSL} - V_{TNL})^2$$

$$K_D[2(v_I - V_{TND})v_O - v_O^2] = K_L(V_{DD} - v_O - V_{TNL})^2$$

the relationship between v_I and v_O in this region is not linear.

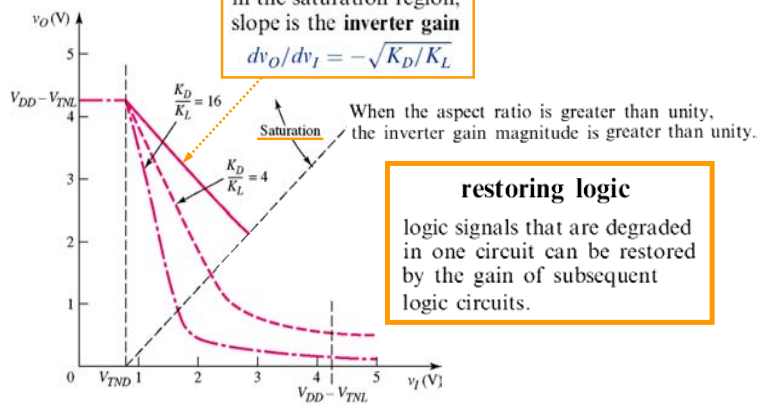
K_D/K_L aspect ratio
width-to-length parameters
of the driver and load transistors.

NMOS Inverter with Enhancement Load



Voltage transfer characteristics, NMOS inverter with saturated load, for three aspect ratios

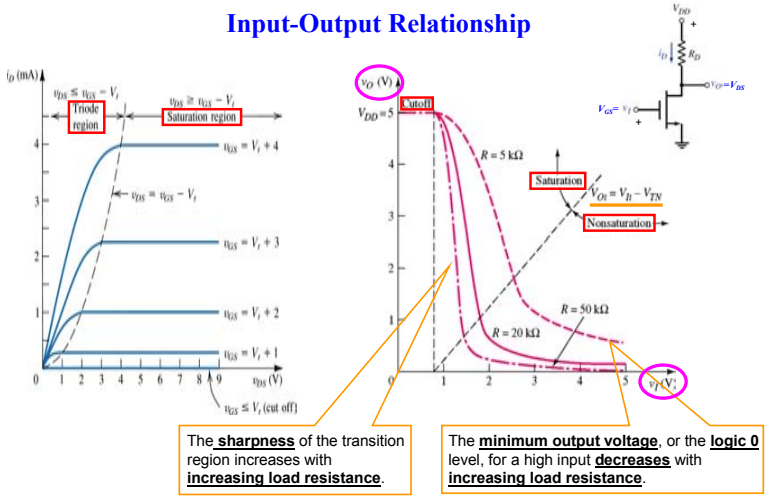
NMOS Inverter with Enhancement Load



Voltage transfer characteristics, NMOS inverter with saturated load, for three aspect ratios

c.f. NMOS Inverter with Resister Load

Input-Output Relationship



The **sharpness** of the transition region increases with **increasing load resistance**.

The **minimum output voltage**, or the **logic 0** level, for a high input **decreases** with **increasing load resistance**.

P1014

Example **Objective:** Design the aspect ratio K_D/K_L to produce a specified low output voltage, and determine the power dissipation in the inverter with enhancement load for a minimum W/L ratio for the load transistor. (Neglect the body effect.)

Consider the inverter shown in Figure 16.8(a) biased at $V_{DD} = 5\,\text{V}$. The transistor parameters are: $V_{TND} = V_{TNL} = 0.8\,\text{V}$ and $k_n' = 35\,\mu\text{A/V}^2$. Determine K_D/K_L such that $v_O = 0.10\,\text{V}$ when $v_I = \text{Logic 1} = 4.2\,\text{V}$, and determine $(W/L)_D$ and the power dissipation in the inverter for $(W/L)_L = 0.5$ and $v_I = 4.2\,\text{V}$.

Limitation of Enhancement Load inverter

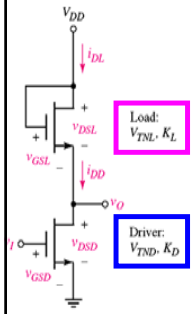
Limitation of Enhancement Load inverter

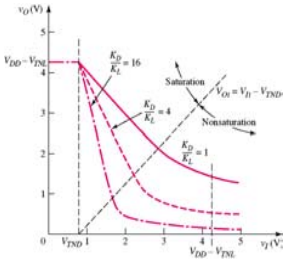
For $v_I = 4.2\,\text{V}$, the driver transistor is in the nonsaturation region.

$$K_D\left[2(v_I - V_{TND})v_O - v_O^2\right] = K_L(V_{DD} - v_O - V_{TNL})^2$$

$$\frac{K_D}{K_L}\left[2(4.2 - 0.8)(0.1) - (0.1)^2\right] = (5 - 0.1 - 0.8)^2 = 25.1$$

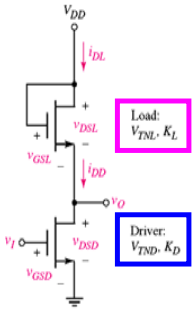
$$\frac{K_D}{K_L} = \frac{(W/L)_D}{(W/L)_L} \qquad (W/L)_D = 12.6 \quad \text{when} \quad (W/L)_L = 0.5$$





Example 16.3 P1014

The power dissipated in the inverter is $P = i_D V_{DD} = (147)(5) = 735\,\mu\text{W}$



from the load transistor,

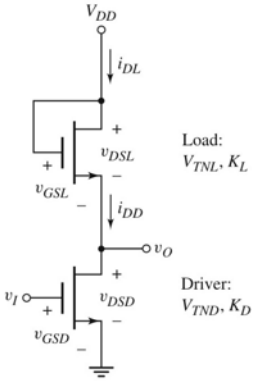
$$i_D = K_L(V_{DD} - v_O - V_{TNL})^2 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_L (V_{DD} - v_O - V_{TNL})^2$$

$$= \left(\frac{35}{2}\right)(0.5)(5 - 0.1 - 0.8)^2 = 147\,\mu\text{A}$$

Comment: In the NMOS inverter with enhancement load, producing a relatively low output voltage V_{OL} requires a large difference in the sizes of the driver and load transistors. The load transistor size cannot be substantially reduced, so the power consumption also cannot be substantially reduced from the 735 μW value. If an IC contained a modest 100,000 inverters and all inverters were conducting, the total required current to the IC would be 14.7 A and the total power dissipated would be 73.5 W!

Example

The enhancement-load NMOS inverter shown in Fig. is biased at V_{DD} = 3 V. The transistor parameters are $V_{TND} = V_{TNL}$ = 0.4 V, k'_n = 60 mA/V², $(W/L)_D$ = 16 and $(W/L)_L$ = 2. (a) Find v_o when (i) v_I = 0, (ii) v_I = 2.6, (b) Calculate the power dissipated in the inverter when v_I = 2.6 V.



EX16.3

(a)

(i)

$$v_o = V_{DD} - V_{TNL} = 3 - 0.4$$

$$v_o = 2.6\ \text{V}$$

(ii)

$$\left(\frac{W}{L}\right)_D\left[2(v_I - 0.4)v_o - v_o^2\right] = \left(\frac{W}{L}\right)_L\left[V_{DD} - v_o - 0.4\right]^2$$

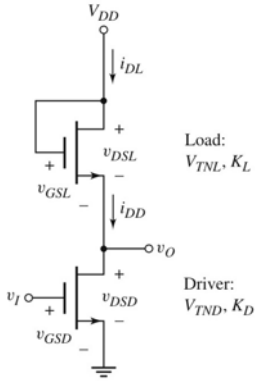
$$16\left[2(2.6 - 0.4)v_o - v_o^2\right] = 2\left[3 - v_o - 0.4\right]^2$$

$$35.2v_o - 8v_o^2 = 6.76 - 5.2v_o + v_o^2$$

$$9v_o^2 - 40.4v_o + 6.76 = 0$$

$$v_o = \frac{40.4 \pm \sqrt{1632.16 - 4(9)(6.76)}}{2(9)}$$

$$v_o = 0.174\ \text{V}$$



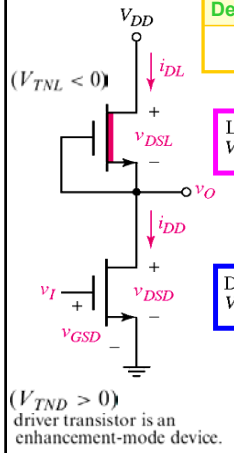
(b)

$$i_D = \left(\frac{60}{2}\right)(2)\left[3 - 0.174 - 0.4\right]^2$$

$$i_D = 353.1\ \mu\text{A}$$

$$P = i_D \cdot V_{DD} = 1.06\ \text{mW}$$

NMOS Inverter with Depletion Load



Depletion mode : Channel exists even with zero gate voltage.

A ***negative* voltage** must be applied to the gate to turn the ***device off.***
Threshold voltage is always *negative*.

Load: V_{TNL}, K_L

Driver: V_{TND}, K_D

- This is an alternate form of the NMOS inverter that uses an **depletion-mode MOSFET load** device with gate and source terminal connected.
- This inverter has the advantage of $V_O = V_{DD}$, as well as more **abrupt** transition region even though the W/L ratio for the output MOSFET is small.

This inverter has been the basis of many microprocessor and static memory designs.

N-Channel Depletion-Mode MOSFET

- In n- channel depletion mode MOSFET, an n-channel region or inversion layer exists under the gate oxide layer even at zero gate voltage and hence term **depletion mode**.
- A negative voltage must be applied to the gate to turn the **device off**.
- The ***threshold voltage*** is always ***negative*** for this kind of device.

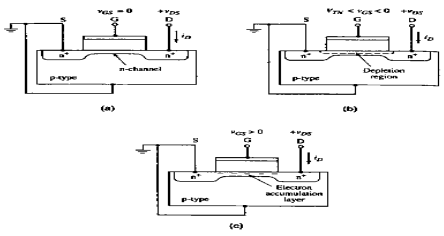


Figure 5.12 Cross section of an n-channel depletion mode MOSFET for: (a) $v_{GS} = 0$, (b) $v_{GS} < 0$, and (c) $v_{GS} > 0$

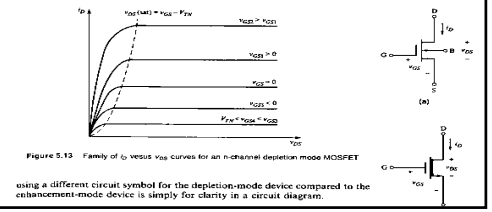
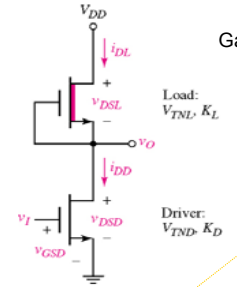


Figure 5.13 Family of i_D versus v_{DS} curves for an n-channel depletion mode MOSFET

using a different circuit symbol for the depletion-mode device compared to the enhancement-mode device is simply for clarity in a circuit diagram.

NMOS Inverter with Depletion Load

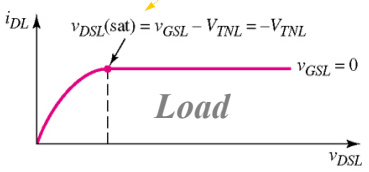


Gate and source are connected, $v_{GSL} = 0$

Since the **threshold voltage** of load transistor is **negative**.

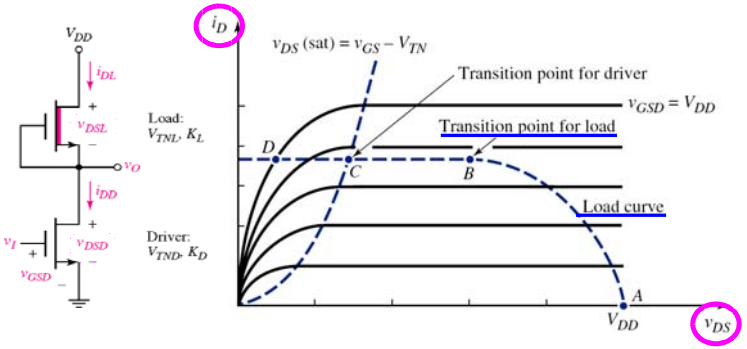
$$v_{DSL}(\text{sat}) = v_{GSL} - V_{TNL} = -V_{TNL}$$

($v_{GSL} = 0$)



NMOS Inverter with Depletion Load

driver transistor characteristics and load curve



NMOS Inverter with Depletion Load (cont.)

Case I: when $V_I < V_{TND}$ (drive is cutoff): No drain current conduct in either transistor. That means the load transistor must be in the linear region of the operation and the output current can be expressed as fellows

$i_{DL}(linear) = K_L[2(V_{GSL} - V_{TNL})V_{DSL} - V_{DSL}^2]$

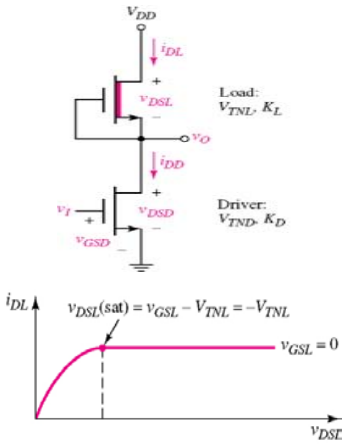
Since $V_{GSL}=0$, and $i_{DL=0}$

$0 = -K_L[2V_{TNL}V_{DSL} + V_{DSL}^2]$

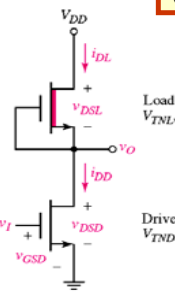
Which gives $\mathbf{V_{DSL}=0}$ **thus**

$\mathbf{V_O = V_{DD}}$

***This is the advantage of the depletion load inverter over the enhancement load inverter*.**



NMOS Inverter with Depletion Load



When $v_I > V_{TND}$ (Just greater than)

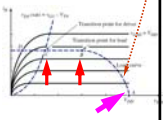
driver turns on and in the saturation region; however, load is in the nonsaturation region. Q-point lies between points A and B

two drain currents equal, $i_{DD} = i_{DL}$

$$K_D[v_{GSD} - V_{TND}]^2 = K_L[2(v_{GSL} - V_{TNL})v_{DSL} - v_{DSL}^2]$$ ($v_{GSL}=0$)

$$K_D[v_I - V_{TND}]^2 = K_L[2(-V_{TNL})(V_{DD} - v_O) - (V_{DD} - v_O)^2]$$

There are two transition points one for the load (B) and one for the driver (C).

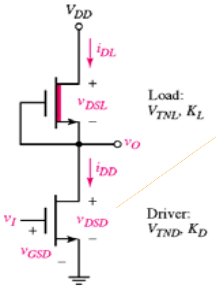


transition point for the load

$$v_{DSL} = V_{DD} - V_{OI} = v_{GSL} - V_{TNL} = -V_{TNL}$$

$V_{OI} = V_{DD} + V_{TNL}$ Since V_{TNL} is negative, the output voltage at the transition point is less than V_{DD}.

NMOS Inverter with Depletion Load



transition point for the driver

$v_{DSD} = v_{GSD} - V_{TND}$ ($v_{DS}(sat) = v_{GS} - V_{TN}$)

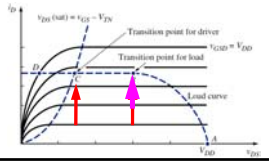
$V_{OI} = V_I - V_{TND}$

When the Q-point lies between points B and C both devices are in the saturation region,

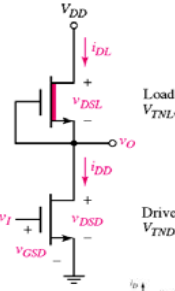
$$K_D(v_{GSD} - V_{TND})^2 = K_L(v_{GSL} - V_{TNL})^2$$

$$\sqrt{\frac{K_D}{K_L}}(v_I - V_{TND}) = -V_{TNL}$$

This implies that input voltage is **constant** as the ***Q*-point passes this region.**



NMOS Inverter with Depletion Load

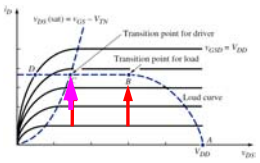


driver is biased in the nonsaturation region while the load is in the saturation region. Q-point is between points C and D

$$K_D[2(v_{GSD} - V_{TND})v_{DSD} - v_{DSD}^2] = K_L(v_{GSL} - V_{TNL})^2$$

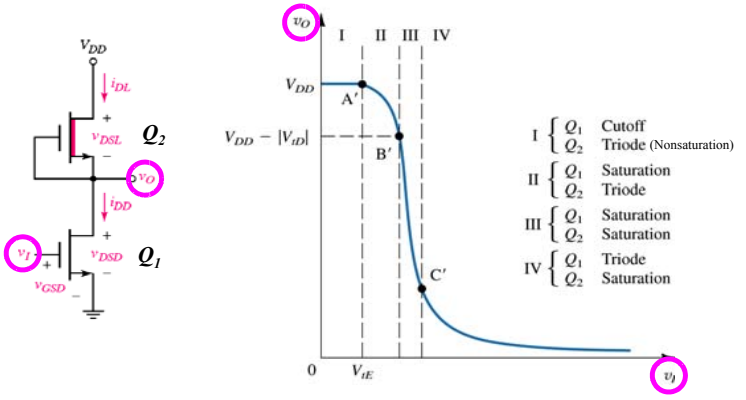
$$\frac{K_D}{K_L}[2(v_I - V_{TND})v_O - v_O^2] = (-V_{TNL})^2$$

This implies that input and output voltages are **not linear** in this region.



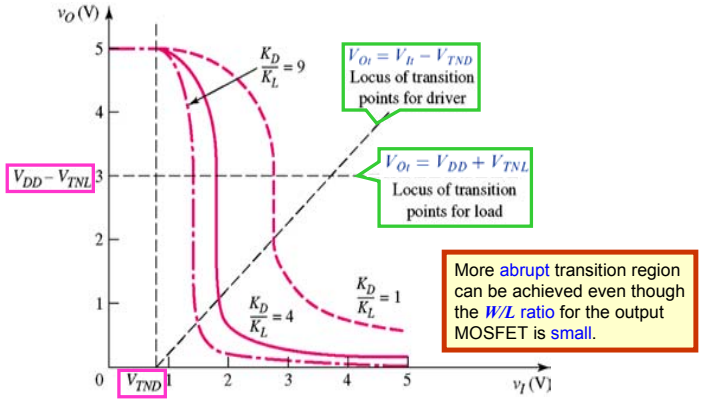
NMOS Inverter with Depletion Load

Voltage transfer characteristics,
NMOS inverter with depletion load,



NMOS Inverter with Depletion Load

Voltage transfer characteristics,
NMOS inverter with depletion load, for three aspect ratios



Example 16.4 P1014

Design Example 16.4 **Objective:** Design the aspect ratio K_D/K_L to produce a specified low output voltage, and determine the power dissipation in the inverter with depletion load for a minimum W/L ratio for the load transistor.

Consider the inverter in Figure 16.10(a) biased at $V_{DD} = 5\,\text{V}$. The transistor parameters are: $V_{TND} = 0.8\,\text{V}$, $V_{TNL} = -2\,\text{V}$, and $k_n' = 35\,\mu\text{A/V}^2$. Determine K_D/K_L such that $v_O = 0.10\,\text{V}$ when $v_I = 5\,\text{V}$. Determine $(W/L)_D$ and the power dissipation in the inverter for $(W/L)_L = 0.5$.

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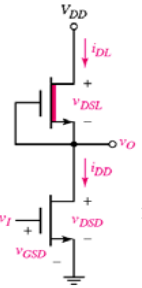

For $v_I = 5\,\text{V}$, we assume the driver transistor is in the nonsaturation region and the load is in the saturation region. (See slide 34)

Load: V_{TNL}, K_L

$$\frac{K_D}{K_L}\left[2(v_I - V_{TND})v_O - v_O^2\right] = (-V_{TNL})^2$$

$$\frac{K_D}{K_L}\left[2(5 - 0.8)(0.1) - (0.1)^2\right] = [-(-2)]^2 = 4.82$$

Driver: V_{TND}, K_D

$$\frac{K_D}{K_L} = \frac{(W/L)_D}{(W/L)_L} \qquad (W/L)_D = 2.41 \text{ when } (W/L)_L = 0.5$$

from the load transistor, (See next slide v_{GS}=0)

$$i_D = K_L(-V_{TNL})^2 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_L(-V_{TNL})^2 = \left(\frac{35}{2}\right)(0.5)[-(-2)]^2 = 35\,\mu\text{A}$$

The power dissipated in the inverter is $P = i_D V_{DD} = (35)(5) = 175\,\mu\text{W}$

Example 16.4 P1014

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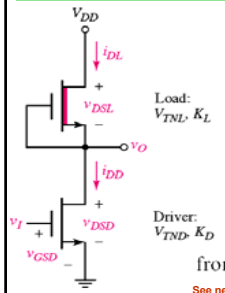


from the load transistor,

See next slide $v_{GS}=0$

$$i_D = K_L(-V_{TNL})^2 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_L(-V_{TNL})^2 = \left(\frac{35}{2}\right)(0.5)[-(-2)]^2 = 35\,\mu\text{A}$$

The power dissipated in the inverter is $P = i_D V_{DD} = (35)(5) = 175\,\mu\text{W}$

Summary of NMOS inverter with Resister Load

Current-Voltage Relationship

Saturation Region

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_I - V_{TN})^2$$

$$v_O = V_{DD} - K_n R_D(v_I - V_{TN})^2$$

Transition Region

$$V_{Ot} = V_{It} - V_{TN}$$

$$K_n R_D(V_{It} - V_{TN})^2 + (V_{It} - V_{TN}) - V_{DD} = 0$$

Nonsaturation Region

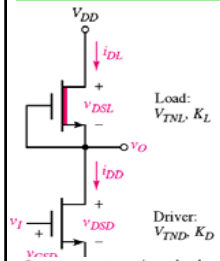
$$i_D = K_n\left[2(v_I - v_{TN})v_O - v_O^2\right]$$

$$v_O = V_{DD} - K_n R_D\left[2(v_I - V_{TN})v_O - v_O^2\right]$$

Example 16.4 P1014

Design Example 16.4 **Objective:** Design the aspect ratio K_D/K_L to produce a specified low output voltage, and determine the power dissipation in the inverter with depletion load for a minimum W/L ratio for the load transistor.

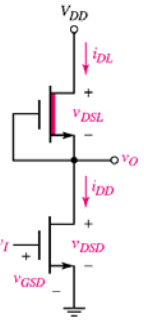
Consider the inverter in Figure 16.10(a) biased at $V_{DD} = 5\,\text{V}$. The transistor parameters are: $V_{TND} = 0.8\,\text{V}$, $V_{TNL} = -2\,\text{V}$, and $k_n' = 35\,\mu\text{A/V}^2$. Determine K_D/K_L such that $v_O = 0.10\,\text{V}$ when $v_I = 5\,\text{V}$. Determine $(W/L)_D$ and the power dissipation in the inverter for $(W/L)_L = 0.5$.



Comment: A relatively low output voltage V_{OL} can be produced in the NMOS inverter with depletion load, even when the load and driver transistors are not vastly different in size. The power dissipation in this inverter is also substantially less than in the enhancement-load inverter since the aspect ratio is smaller.

Design 16.5 P1018

D16.5 Consider the depletion load inverter in Figure 16.10(a) biased at $V_{DD} = 5\,\text{V}$. The threshold voltages are $V_{TND} = 0.8\,\text{V}$ and $V_{TNL} = -2\,\text{V}$. Design the inverter such that the maximum power dissipation is $350\,\mu\text{W}$ and the output voltage is $0.05\,\text{V}$ when $v_I = 5\,\text{V}$. (Ans. $(W/L)_L = 1$, $(W/L)_D = 9.58$)



Design 16.5 P1018

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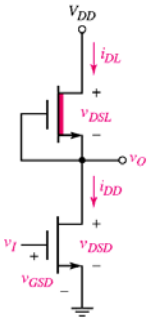


$P = i_D V_{DD}$

$350 = i_D \cdot 5 \Rightarrow i_D = \frac{350}{5} = 70\,mA$

$i_D = 70\,mA$ (Load)

Since gate to source terminal of the load transistor are short

$\Rightarrow V_{GSL} = 0$, which is much greater than V_{TNL}

Load transistor is in Saturation mode

$i_D = K_L (V_{GSL} - V_{TNL})^2$

Since $V_{GSL} = 0$

$i_D = K_L (V_{GSL} - V_{TNL})^2 = K_L (-V_{TNL})^2$

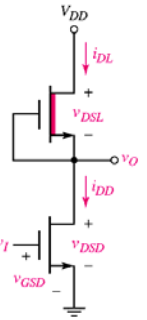
$i_D = \left(\frac{K_n'}{2}\right)\left(\frac{W}{L}\right)_L (-V_{TNL})^2$

$70 = \left(\frac{35}{2}\right)\left(\frac{W}{L}\right)_L (-(-2))^2$

$\left(\frac{W}{L}\right)_L = 1$

Design 16.5 P1018

D16.5 Consider the depletion load inverter in Figure 16.10(a) biased at $V_{DD} = 5\,V$. The threshold voltages are $V_{TND} = 0.8\,V$ and $V_{TNL} = -2\,V$. Design the inverter such that the maximum power dissipation is $350\,\mu W$ and the output voltage is $0.05\,V$ when $v_I = 5\,V$. (Ans. $(W/L)_L = 1$, $(W/L)_D = 9.58$)



Also we have

$V_I = 5V$ and $V_o = 0.05\,V$ for Driver

$\Rightarrow$ Driver must be in nonsaturation mode

$\Rightarrow i_D = K_D\left[2(V_{GSD} - V_{TND})V_{DSD} - V_{DSD}^2\right]$

or $i_D = K_D\left[2(V_I - V_{TND})V_o - V_o^2\right]$

Substituting given values

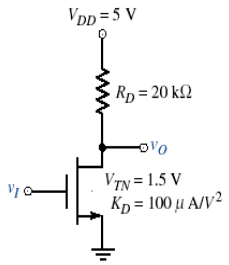
$70 = \frac{K_n'}{2}\left(\frac{W}{L}\right)_D [\quad ----]$

$70 = \frac{35}{2}\left(\frac{W}{L}\right)_D \left[2(5 - 0.8)0.05 - (0.05)^2\right]$

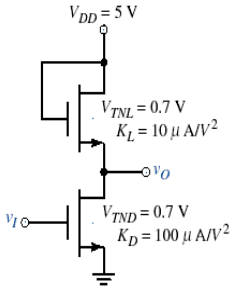
$70 = 7.31\left(\frac{W}{L}\right)_D$

$\Rightarrow \left(\frac{W}{L}\right)_D = 9.58$

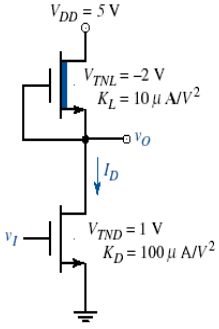
16.14 Calculate the power dissipated in each inverter circuit in Figure P16.14 for the following input conditions: (a) Inverter a: (i) $v_I = 0.5\,V$, (ii) $v_I = 5\,V$; (b) Inverter b: (i) $v_I = 0.25\,V$, (ii) $v_I = 4.3\,V$; (c) Inverter c: (i) $v_I = 0.03\,V$, (ii) $v_I = 5\,V$.



(a)



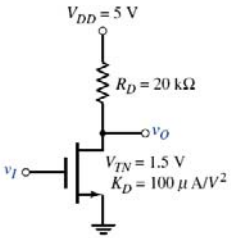
(b)



(c)

Example 16.14 P1098

16.14 Calculate the power dissipated in each inverter circuit in Figure P16.14 for the following input conditions: (a) Inverter a: (i) $v_I = 0.5\,V$, (ii) $v_I = 5\,V$; (b) Inverter b: (i) $v_I = 0.25\,V$, (ii) $v_I = 4.3\,V$; (c) Inverter c: (i) $v_I = 0.03\,V$, (ii) $v_I = 5\,V$.



(a)

(i) $v_I = 0.5\,V \Rightarrow i_D = 0 \Rightarrow \underline{P = 0}$

(ii) $v_I = 5\,V$, **From Equation (16.12),**

nonsaturation region

$v_O = V_{DD} - K_n R_D\left[2(v_I - V_{TN})v_O - v_O^2\right]$

$v_o = 5 - (0.1)(20)\left[2(5 - 1.5)v_o - v_o^2\right]$

$2v_o^2 - 15v_o + 5 = 0$

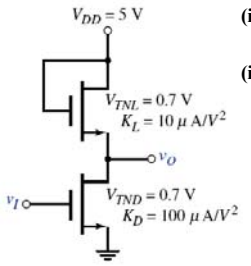
$v_o = \frac{15 \pm \sqrt{(15)^2 - 4(2)(5)}}{2(2)} \Rightarrow \underline{v_o = 0.35\,V}$

$i_D = \frac{5 - 0.35}{20} = 0.2325\,mA$

$P = i_D \cdot V_{DD} = (0.2325)(5) \Rightarrow \underline{P = 1.16\,mW}$

Example 16.14 P1098

16.14 Calculate the power dissipated in each inverter circuit in Figure P16.14 for the following input conditions: (a) Inverter a: (i) $v_I = 0.5$ V, (ii) $v_I = 5$ V; (b) Inverter b: (i) $v_I = 0.25$ V, (ii) $v_I = 4.3$ V; (c) Inverter c: (i) $v_I = 0.03$ V, (ii) $v_I = 5$ V.



(b)

(i) $v_I = 0.25$ V $\Rightarrow i_D = 0 \Rightarrow \underline{P = 0}$

(ii) $v_I = 4.3$ V, From Equation (16.23),

input voltage greater than V_{It}

$$K_D\left[2(v_I - V_{TND})v_O - v_O^2\right] = K_L(V_{DD} - v_O - V_{TNL})^2$$

$$100\left[2(4.3 - 0.7)v_O - v_O^2\right] = 10[5 - v_O - 0.7]^2$$

$$10\left[7.2v_O - v_O^2\right] = 18.49 - 8.6v_O + v_O^2$$

$$11v_O^2 - 80.6v_O + 18.49 = 0$$

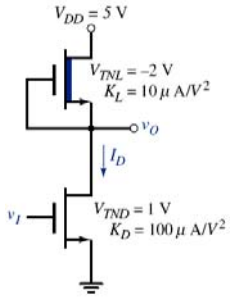
$$v_O = \frac{80.6 \pm \sqrt{(80.6)^2 - 4(11)(18.49)}}{2(11)} = \underline{0.237\text{ V}}$$

$$i_D = 10[5 - 0.237 - 0.7]^2 = 165\ \mu\text{A}$$

$$P = i_D \cdot V_{DD} = (165)(5) \Rightarrow \underline{P = 825\ \mu\text{W}}$$

Example 16.14 P1098

16.14 Calculate the power dissipated in each inverter circuit in Figure P16.14 for the following input conditions: (a) Inverter a: (i) $v_I = 0.5$ V, (ii) $v_I = 5$ V; (b) Inverter b: (i) $v_I = 0.25$ V, (ii) $v_I = 4.3$ V; (c) Inverter c: (i) $v_I = 0.03$ V, (ii) $v_I = 5$ V.



(c)

(i) $v_I = 0.03$ V $\Rightarrow i_D = 0 \Rightarrow \underline{P = 0}$

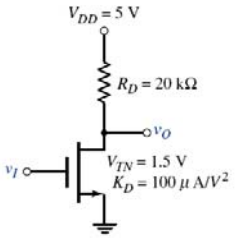
(ii) $v_I = 5$ V

$$i_D = K_L(-V_{TNL})^2 = (10)[-(-2)]^2 = 40\ \mu A$$

$$P = i_D \cdot V_{DD} = (40)(5) \Rightarrow \underline{P = 200\ \mu\text{W}}$$

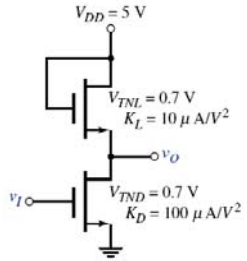
Example 16.14 P1098

NMOS Inverter



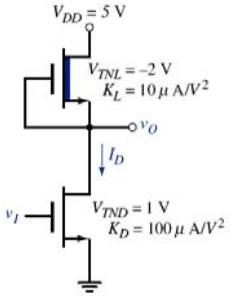
(a)

1160μW
Resister Load



(b)

825μW
Enhancement Load



(c)

200μW
Depletion Load

Chapter 16

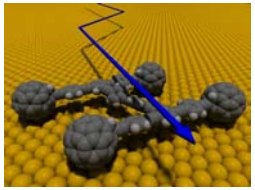
MOSFET Digital Circuits

Chapter 16.2

NMOS Logic Circuit

NMOS Logic Circuit

NMOS logic circuits are constructed by connecting driver transistor in **parallel, series** or **series-parallel combinations** to produce required output logic function



Logic Gates

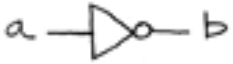
AND

ab	c
00	0
01	0
10	0
11	1

OR

ab	c
00	0
01	1
10	1
11	1

NOT



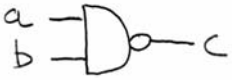
a	b
0	1
1	0

Logic Gates

XOR

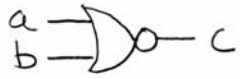
ab	c
00	0
01	1
10	1
11	0

NAND



ab	c
00	1
01	1
10	1
11	0

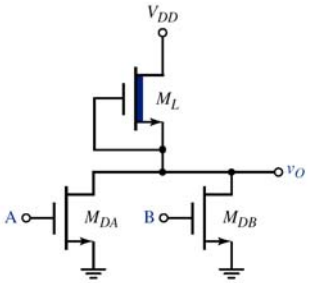
NOR



ab	c
00	1
01	0
10	0
11	0

NMOS NOR Gate

- NMOS NOR gate can be constructed by connecting an additional **driver transistor** in parallel with a **depletion load inverter**.

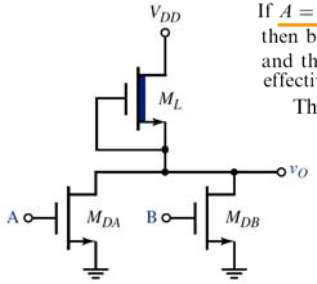


Two-input NMOS NOR logic gate with depletion load

If $A = B =$ logic 0,
then both M_{DA} and M_{DB} are cut off
and $v_O = V_{DD}$.

If $A =$ logic 1 and $B =$ logic 0,
then M_{DB} is cut off
and the NMOS inverter with M_L and M_{DA}
if $A =$ logic 0 and $B =$ logic 1,
same inverter configuration.

NMOS NOR Gate



Two-input NMOS NOR logic gate with depletion load

If $A = B =$ logic 1, then both M_{DA} and M_{DB} turn on and the two driver transistors are effectively in parallel.

The value of the output voltage changes slightly.

$$i_{DL} = i_{DA} + i_{DB}$$

$$K_L[v_{GSL} - V_{TNL}]^2 = K_{DA}[2(v_{GSA} - V_{TNA})v_{DSA} - v_{DSA}^2] + K_{DB}[2(v_{GSB} - V_{TNB})v_{DSB} - v_{DSB}^2]$$

If transistors are identical,

$$K_{DA} = K_{DB} \equiv K_D \quad V_{TNA} = V_{TNB} \equiv V_{TND}$$

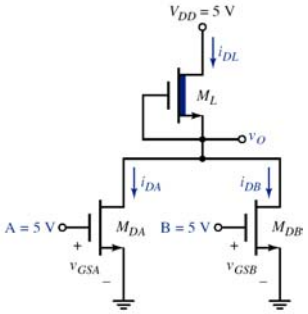
$$v_{GSL} = 0,\ v_{GSA} = v_{GSB} = V_{DD},\ v_{DSA} = v_{DSB} = v_O$$

$$[-V_{TNL}]^2 = 2\left(\frac{K_D}{K_L}\right)[2(V_{DD} - V_{TND})v_O - v_O^2]$$

when both drivers are conducting, the effective width-to-length ratio of the composite driver transistor doubles.
the output voltage becomes slightly smaller when both inputs are high.

NMOS NOR Gate

When all Inputs are at logic 1



When A = B = logic 1

Both driver transistors are switched into nonsaturation region and load transistor is biased in saturation region.

$$i_{DL} = i_{DA} + i_{DB}$$

$$K_L[v_{GSL} - V_{TNL}]^2 = K_{DA}[2(v_{GSA} - V_{TNA})v_{DSA} - v_{DSA}^2] + K_{DB}[2(v_{GSB} - V_{TNB})v_{DSB} - v_{DSB}^2]$$

Suppose two driver transistors are identical,
$K_{DA} = K_{DB} \equiv K_D \quad V_{TNA} = V_{TNB} \equiv V_{TND}$
$v_{GSL} = 0,\ v_{GSA} = v_{GSB} = V_{DD},\ v_{DSA} = v_{DSB} = v_O$

$$[-V_{TNL}]^2 = 2\left(\frac{K_D}{K_L}\right)[2(V_{DD} - V_{TND})v_O - v_O^2]$$

when both drivers are conducting, the effective width-to-length ratio of the composite driver transistor doubles.

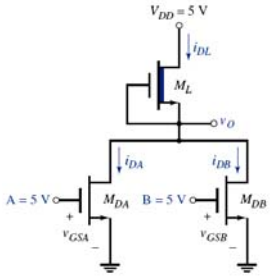
This means that the output voltage becomes slightly smaller when both inputs are high.

higher the aspect ratio lower the output.

Example 16.7 p1030

Example 16.7 **Objective:** Determine the low output voltage of an NMOS NOR circuit.

Consider the NOR circuit in Figure 16.24 biased at $V_{DD} = 5$ V. Assume that $k_n' = 35\ \mu A/V^2$. Also assume the width-to-length ratios of the load and driver transistors are $(W/L)_L = 1$ and $(W/L)_D = 4$, respectively. Let $V_{TND} = 0.8$ V and $V_{TNL} = -2$ V. Neglect the body effect.



Two-input NMOS NOR logic gate

If, $A =$ logic 1 $= 5$ V and $B =$ logic 0, then M_{DB} is cut off.

$$\frac{K_D}{K_L}[2(v_I - V_{TND})v_O - v_O^2] = (-V_{TNL})^2$$

$$\frac{K_D}{K_L}[2(v_I - V_{TND})v_O - v_O^2] = (-V_{TNL})^2 \qquad \left(\frac{4}{1}\right)[2(5 - 0.8)v_O - v_O^2] = (2)^2$$

$$v_O = 0.121\ \text{V}$$

If both inputs go high,

$$A = B = V_{DD} = 5\ \text{V}$$

$$[-V_{TNL}]^2 = 2\left(\frac{K_D}{K_L}\right)[2(V_{DD} - V_{TND})v_O - v_O^2]$$

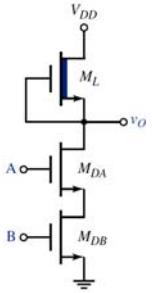
$$[-V_{TNL}]^2 = 2\left(\frac{K_D}{K_L}\right)[2(V_{DD} - V_{TND})v_O - v_O^2]$$

$$(2)^2 = 2\left(\frac{4}{1}\right)[2(5 - 0.8)v_O - v_O^2]$$

$$v_O = 0.060\ \text{V}$$

NMOS NAND Gate

Additional driver transistor connected in Series



Two-input NMOS NAND logic gate with depletion load

If both $A = B =$ logic 0, or if either A or B is a logic 0, at least one driver is cut off, and the output is high.

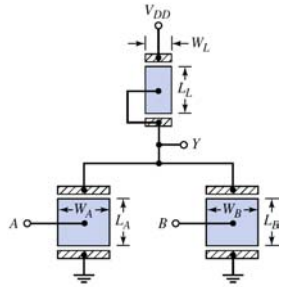
If both $A = B =$ logic 1, then the composite driver of the NMOS inverter conducts and the output goes low.

Since the gate-to-source voltages of M_{DA} and M_{DB} are not equal, determining the actual voltage V_{OL} of a NAND gate is difficult. The drain-to-source voltages of M_{DA} and M_{DB} must adjust themselves to produce the same current.

NMOS Logic Circuit

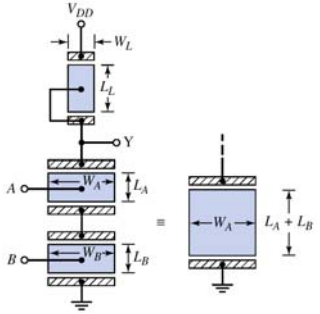
Concept of Effective Width-to-Length Ratios

Parallel combination



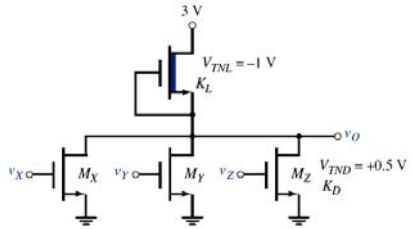
For the **NOR gate** the **effective width of the drivers transistors doubles.**
The effective aspect ratio is increased.

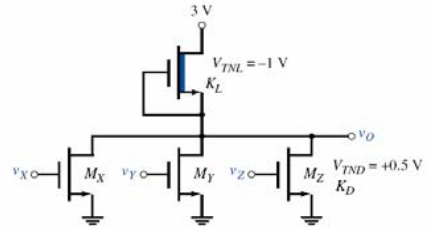
Series combination



For the **NAND gate** the **effective length of the driver transistors doubles.**
The effective aspect ratio is decreased.

D16.20 Consider the three-input NOR logic gate in Figure P16.20. The transistor parameters are $V_{TNL} = -1$ V and $V_{TND} = 0.5$ V. The maximum value of v_O in its low state is to be 0.1 V. (a) Determine K_D/K_L. (b) The maximum power dissipation in the NOR logic gate is to be 0.1 mW. Determine the width-to-length ratios of the transistors. (c) Determine v_O when $v_X = v_Y = v_Z = 3$ V.





(a) **Maximum value of v_o in low state- when only one input is high, then,** $\frac{K_D}{K_L}[2(v_I - V_{TND})v_O - v_O^2] = (-V_{TNL})^2$

$$\frac{K_D}{K_L}\left[2(3-0.5)(0.1)-(0.1)^2\right] = \left[-(-1)\right]^2 = 2.04$$

(b) $P = i_D \cdot V_{DD}$

$$0.1 = i_D(3) \Rightarrow i_D = 33.3\ \mu A$$

$$i_D = \left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)_L (-V_{TNL})^2$$

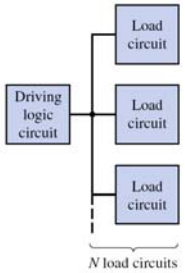
$$33.3 = \left(\frac{80}{2}\right)\left(\frac{W}{L}\right)_L \left[-(-1)\right]^2 \Rightarrow \left(\frac{W}{L}\right)_L = 0.8325$$

$$\left(\frac{W}{L}\right)_D = 1.70$$

(c) $[-V_{TNL}]^2 = 2\left(\frac{K_D}{K_L}\right)[2(V_{DD} - V_{TND})v_O - v_O^2]$

$$3(2.04)\left[2(3-0.5)v_o - v_o^2\right] = \left[-(-1)\right]^2 \Rightarrow v_o = 0.0329\ V$$

Fan-In and Fan-Out



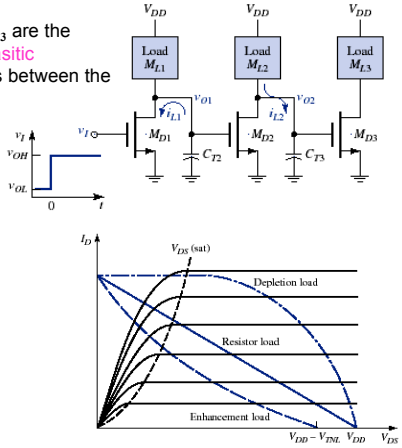
Logic circuit driving *N* load circuits

- The **Fan-in** of a gate is the number of its inputs. Thus a four input NOR gate has a fan-in of 4.
- Similarly, **Fan-Out** is the maximum number of similar gates that a gate can drive while remaining within guaranteed specifications.

dc characteristics of MOS logic circuits are unaffected by the fanout to other MOS logic inputs. However, the load capacitance due to a large fanout seriously degrades the switching speed and propagation delay times. Consequently, maintaining the propagation delay time below a specified maximum value determines the fanout of MOS digital circuits.

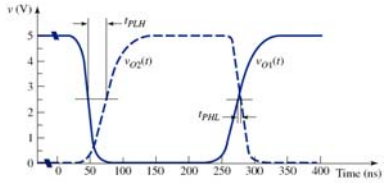
Transient Analysis of NMOS Inverters

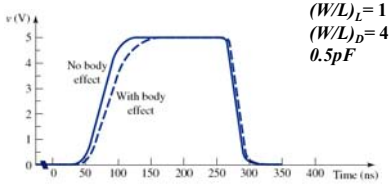
- The source of capacitance C_{T2} and C_{T3} are the transistor input capacitances and parasitic capacitances due to interconnect lines between the inverter stages.
- The constant current over a wide range of V_{DS} provided by the depletion load implies that this type of inverter switch a capacitive load more rapidly than the other two types inverter configurations.



The rate at which the voltage across a load capacitance changes is a direct function of the current through the capacitance.

Transient Analysis of NMOS Inverters





$(W/L)_L = 1$
$(W/L)_D = 4$
$0.5pF$

- The **raise time** is longer because the load capacitor is charged by the current through the smaller load transistor.
- The **fall time** relatively short, because the load capacitor discharges through the large driver transistor.

Switching characteristics of an NMOS inverter with depletion load

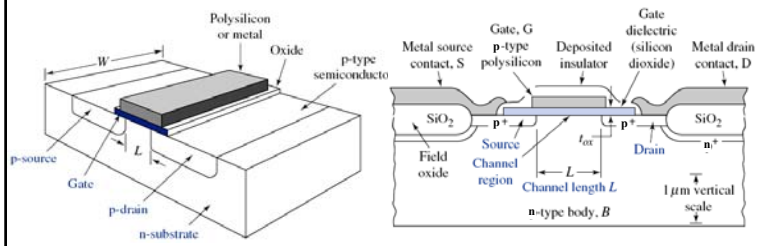
Chapter 16

MOSFET Digital Circuits

Chapter 16.3

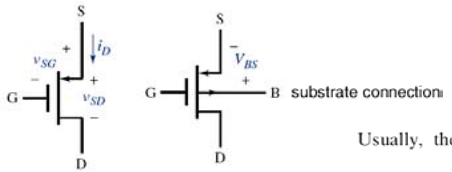
CMOS Inverter

p-Channel MOSFET



the channel length is the same for all transistors, while the channel width is variable.

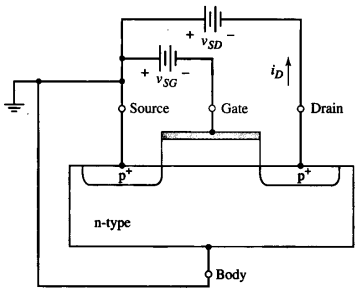
p-channel enhancement-mode MOSFET



Usually, the p-channel depletion-mode device is not used in CMOS digital circuits

p-Channel MOSFET

- In p-channel enhancement device. A negative gate-to-source voltage must be applied to create the inversion layer, or **channel region**, of holes that, "connect" the source and drain regions.
- The **threshold voltage** V_{TP} for p-channel **enhancement-mode** device is alway[illegible] **n-mode** PMOS.



Cross-section of p-channel enhancement mode MOSFET

Summary of Transistor Operation

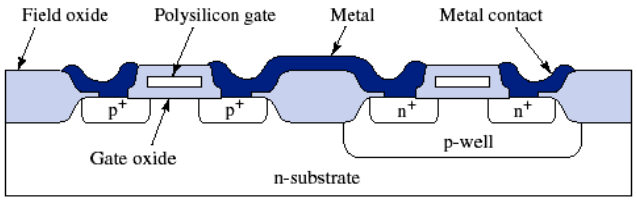
NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

CMOS

Complementary MOS

The most abundant devices on earth

- Although the processing is more complicated for CMOS circuits than for NMOS circuits, CMOS has replaced NMOS at all level of integration, in both analog and digital applications.
- The basic reason of this replacement is that the power dissipation in CMOS logic circuits is much less than in NMOS circuits.



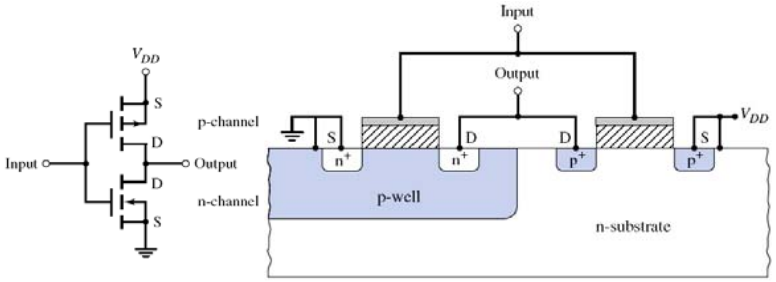
CMOS Properties

- Full rail-to-rail swing ➔ high noise margins
  - Logic levels not dependent upon the relative device sizes ➔ transistors can be minimum size ➔ ratio less
- Always a path to V_{DD} or GND in steady state ➔ low output impedance (output resistance in kΩ range) ➔ large fan-out.
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) ➔ nearly zero steady-state input current
- No direct path steady-state between power and ground ➔ no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors

CMOS Inverter

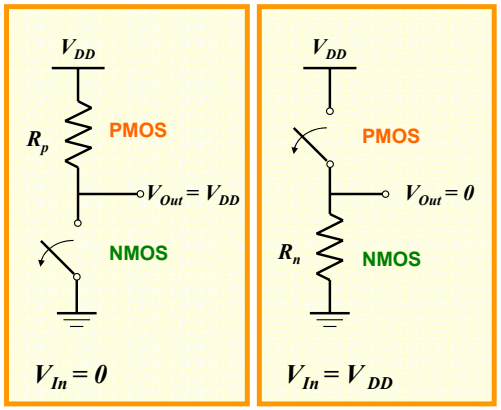
- In the fabrication process, a separate **p-well** region is formed within the starting n-substrate.
- The n-channel MOSFET is fabricated in the p-well region and p-channel MOSFET is fabricated in the n-substrate.

a series combination of a p-channel and an n-channel MOSFET.



CMOS Inverter

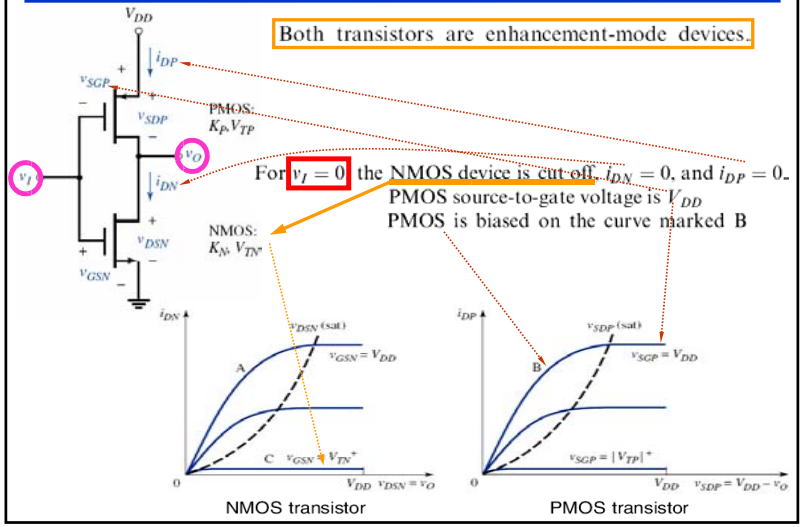
Steady State Response



$$V_{OL} = 0$$
$$V_{OH} = V_{DD}$$

DC Analysis of the CMOS Inverter

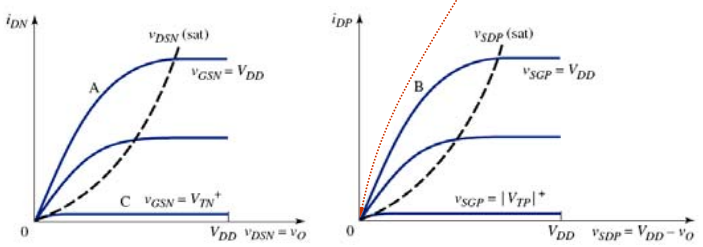
Both transistors are enhancement-mode devices.



DC Analysis of the CMOS Inverter

For $v_I = 0$ the NMOS device is cut off, $i_{DN} = 0$, and $i_{DP} = 0$.
PMOS source-to-gate voltage is V_{DD}
PMOS is biased on the curve marked B

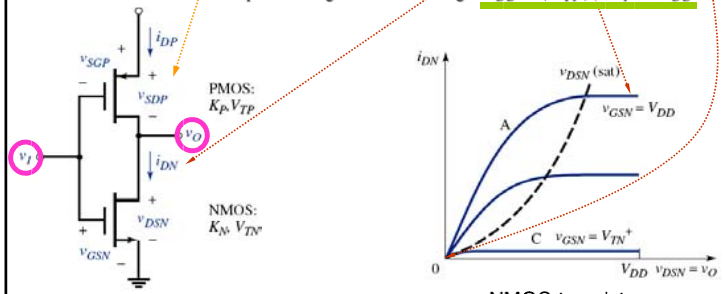
Since the only point on the curve corresponding to $i_{DP} = 0$ occurs at $v_{SDP} = 0 = V_{DD} - v_O$, the output voltage is $v_O = V_{DD}$. This condition exists as long as the NMOS transistor is cut off, or $v_I \le V_{TN}$.



NMOS transistor PMOS transistor

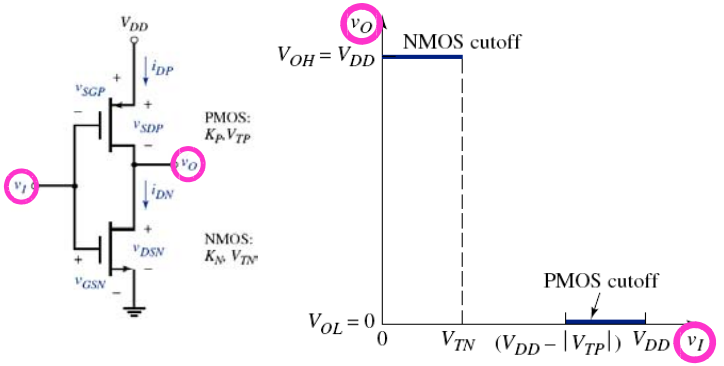
DC Analysis of the CMOS Inverter

For $v_I = V_{DD}$, the PMOS device is cut off, $i_{DP} = 0$, and $i_{DN} = 0$.
NMOS gate-to-source voltage is V_{DD}
NMOS is biased on the curve marked A.
The only point on the curve corresponding to $i_{DN} = 0$ occurs at $v_{DSN} = v_O = 0$.
The output voltage is zero as long as the PMOS transistor is cut off,
or $v_{SGP} = V_{DD} - v_I \le |V_{TP}|$,
input voltage is in the range $V_{DD} - |V_{TP}| \le v_I \le V_{DD}$.



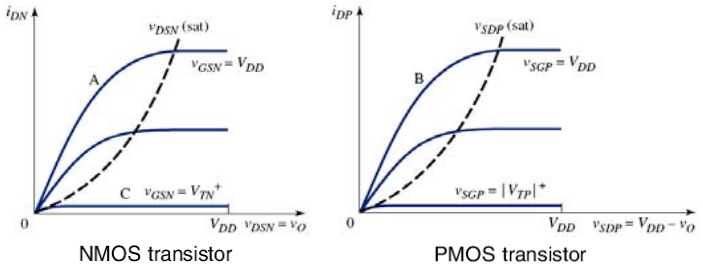
NMOS transistor

DC Analysis of the CMOS Inverter



CMOS inverter output voltage for input voltage in either high state or low state

DC Analysis of the CMOS Inverter



NMOS transistor PMOS transistor

Voltage Transfer Curve

EX16.2

(a)

$$v_o = V_{DD} - I_D R_D$$

$$v_o = 3 - \left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)\left[2(3-0.5)v_o - v_o^2\right]R_D$$

$$v_o = 0.1$$

$$0.1 = 3 - \left(\frac{0.06}{2}\right)(5)\left[(5)(0.1) - (0.1)^2\right]R_D$$

$$0.1 = 3 - 0.0735R_D$$

$$R_D = 39.5 \text{ K}$$

(b)

$$\left(\frac{0.06}{2}\right)(5)(39.5)(V_{It} - 0.5)^2 + (V_{It} - 0.5) - 3 = 0$$

$$5.925(V_{It} - 0.5)^2 + (V_{It} - 0.5) - 3 = 0$$

$$(V_{It} - 0.5) = V_{Ot} = \frac{-1 \pm \sqrt{1 + 4(5.925)(3)}}{2(5.925)}$$

$$V_{Ot} = 0.632 \text{ V}$$

$$V_{It} = 1.132 \text{ V}$$

16.6

(a) From Equation (16.23)

$$\frac{K_D}{K_L}\left[2(3-0.5)(0.25) - (0.25)^2\right] = (3 - 0.25 - 0.5)^2 \Rightarrow \underline{\frac{K_D}{K_L} = 4.26}$$

(b)

$$\frac{K_D}{K_L}\left[2(2.5-0.5)(0.25) - (0.25)^2\right] = (3 - 0.25 - 0.5)^2 \Rightarrow \underline{\frac{K_D}{K_L} = 5.4}$$

(c)

$$i_D = K_L\left(V_{GSL} - V_{TNL}\right)^2 = K_L(V_{DD} - v_O - V_{TNL})^2$$

$$= \left(\frac{0.080}{2}\right)(1)(3 - 0.25 - 0.5)^2 \Rightarrow \underline{i_D = 0.203\ mA}$$

$$P = i_D \cdot V_{DD} = (0.203)(3) \Rightarrow \underline{P = 0.608\ mW}$$

for both parts (a) and (b).

HW solution

16.4

$$0.25 = I(33) \Rightarrow I = 75.76\ \mu\text{A}$$

$$R = \frac{3.3 - 0.15}{0.07576} \Rightarrow \underline{R = 41.6 \text{ K}}$$

$$I = \left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2$$

$$75.76 = \left(\frac{80}{2}\right)\left(\frac{W}{L}\right)(3.3 - 0.8)^2 \Rightarrow \underline{\left(\frac{W}{L}\right) = 0.303}$$

(b)

$$V_{DS}(\text{sat}) = V_{GS} - V_{TN}$$

$$I_D = K_n\left(V_{GS} - V_{TN}\right)^2 = \frac{V_{DD} - V_{DS}(\text{sat})}{R}$$

$$\left(\frac{0.08}{2}\right)(0.303)\left(V_{GS}^2 - 1.6V_{GS} + 0.64\right) = \frac{3.3 - (V_{GS} - 0.8)}{41.6}$$

$$0.504\left(V_{GS}^2 - 1.6V_{GS} + 0.64\right) = 4.1 - V_{GS}$$

$$0.504V_{GS}^2 + 0.1936V_{GS} - 3.777 = 0$$

$$V_{GS} = \frac{-0.1936 \pm \sqrt{0.03748 + 4(0.504)(3.777)}}{2(0.504)}$$

$$V_{GS} = 2.55 \text{ V}$$

For $0.8 \le V_{GS} \le 2.55$ V

Transistor biased in saturation region

16.9

$V_{OH} = V_B - V_{TN} = \text{Logic 1}$

So

(a) $V_B = 4\ V \Rightarrow V_{OH} = 3\ V$

(b) $V_B = 5\ V \Rightarrow V_{OH} = 4\ V$

(c) $V_B = 6\ V \Rightarrow V_{OH} = 5\ V$

(d) $V_B = 7\ V \Rightarrow V_{OH} = 5\ V$, since $V_{DS} = 0$

For $v_I = V_{OH}$

$$K_D\left[2\left(v_I - V_T\right)v_O - v_O^2\right] = K_L\left[V_B - v_O - V_T\right]^2$$

Then

(a) $$(1)\left[2(3-1)V_{OL} - V_{OL}^2\right] = (0.4)\left[4 - V_{OL} - 1\right]^2 \Rightarrow \underline{V_{OL} = 0.657\ V}$$

(b) $$(1)\left[2(4-1)V_{OL} - V_{OL}^2\right] = (0.4)\left[5 - V_{OL} - 1\right]^2 \Rightarrow \underline{V_{OL} = 0.791\ V}$$

(c) $$(1)\left[2(5-1)V_{OL} - V_{OL}^2\right] = (0.4)\left[6 - V_{OL} - 1\right]^2 \Rightarrow \underline{V_{OL} = 0.935\ V}$$

(d) Load in non-sat region

$i_{DD} = i_{DL}$

(1) $\left[2(5-1)V_{OL} - V_{OL}^2\right] = (0.4)\left[2(7-V_{OL}-1)(5-V_{OL}) - (5-V_{OL})^2\right]$

$8V_{OL} - V_{OL}^2 = (0.4)\left[2(6-V_{OL})(5-V_{OL}) - (25-10V_{OL}+V_{OL}^2)\right]$

$= (0.4)\left[2(30-11V_{OL}+V_{OL}^2) - 25 + 10V_{OL} - V_{OL}^2\right]$

$= (0.4)\left[60 - 22V_{OL} + 2V_{OL}^2 - 25 + 10V_{OL} - V_{OL}^2\right]$

$8V_{OL} - V_{OL}^2 = 14 - 4.8V_{OL} + 0.4V_{OL}^2$

$1.4V_{OL}^2 - 12.8V_{OL} + 14 = 0$

$$V_{OL} = \frac{12.8 \pm \sqrt{163.84 - 4(1.4)(14)}}{2(1.4)}$$

$V_{OL} = 1.27V$

For load

$V_{DS}(\text{sat}) = 7 - 1.27 - 1 = 4.73V$

$V_{DS} = 5 - 1.27 = 3.73$ non-sat

16.12

(a)

$P = i_D \cdot V_{DD}$

$150 = i_D \cdot (3) \Rightarrow i_D = 50\ \mu A$

$i_D = K_L(-V_{TNL})^2$

$50 = \left(\frac{80}{2}\right)\left(\frac{W}{L}\right)_L \left[-(-1)\right]^2 \Rightarrow \underline{\left(\frac{W}{L}\right)_L = 1.25}$

$\frac{K_D}{K_L}\left[2(3-0.5)(0.1) - (0.1)^2\right] = \left[-(-1)\right]^2$

$\frac{K_D}{K_L} = \frac{(W/L)_D}{(W/L)_L} = 2.04 \Rightarrow \underline{\left(\frac{W}{L}\right)_D = 2.55}$

For the Load:

$V_{Ot} = V_{DD} + V_{TNL} = 3 - 1 \Rightarrow \underline{V_{Ot} = 2\ V}$

$\sqrt{2.04}\,(V_{It} - 0.5) = \left[-(-1)\right] \Rightarrow \underline{V_{It} = 1.20\ V}$

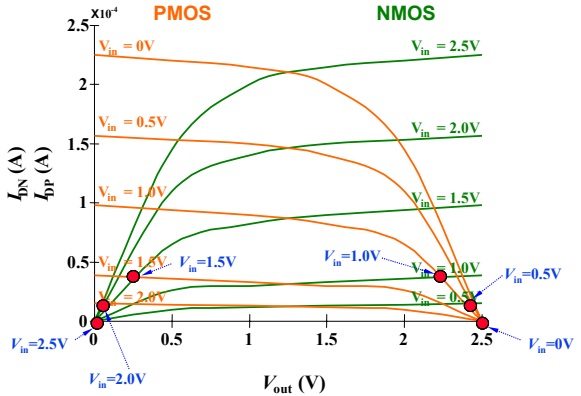
For the Driver:

$V_{Ot} = V_{It} - V_{TND} = 1.20 - 0.5 \Rightarrow \underline{V_{Ot} = 0.70\ V}$

$\underline{V_{It} = 1.20\ V}$

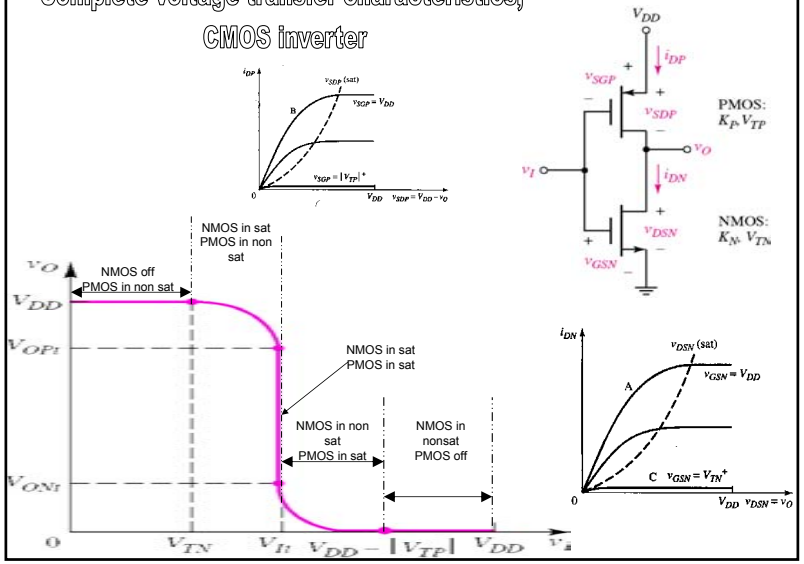
DC Analysis of the CMOS Inverter

CMOS Inverter Load Lines

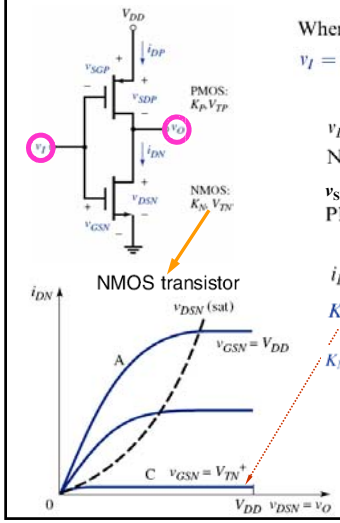


0.25um, W/L_n = 1.5, W/L_p = 4.5, V_{DD} = 2.5V, V_{Tn} = 0.4V, V_{Tp} = -0.4V

Complete voltage transfer characteristics, CMOS inverter



DC Analysis of the CMOS Inverter



When the input voltage is just greater than V_{TN}

$v_I = v_{GSN} = V_{TN}^+$ NMOS begins to conduct
Q-point falls on the curve C

$v_{DSN} \cong V_{DD}$
NMOS is biased in the saturation region

v_{SDP} is small
PMOS is biased in the nonsaturation region.

$i_{DN} = i_{DP}$

$$K_N[v_{GSN} - V_{TN}]^2 = K_P[2(v_{SGP} + V_{TP})v_{SDP} - v_{SDP}^2]$$

$$K_N[v_I - V_{TN}]^2 = K_P[2(V_{DD} - v_I + V_{TP})(V_{DD} - v_O) - (V_{DD} - v_O)^2]$$

v_I and v_O relationship as long as
NMOS: saturation, PMOS: nonsaturation

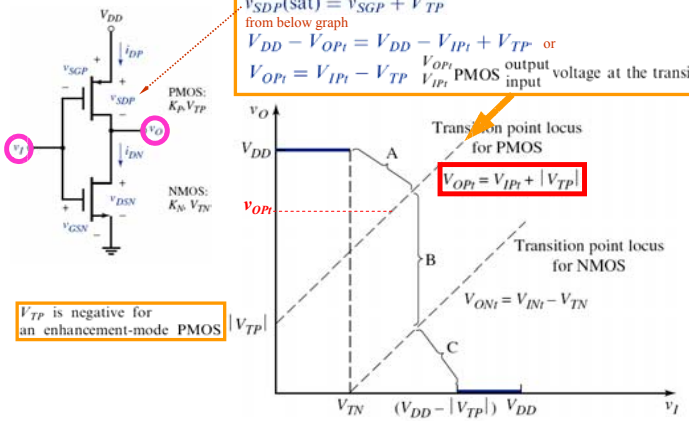
DC Analysis of the CMOS Inverter

The transition point for the PMOS

$v_{SDP}(\text{sat}) = v_{SGP} + V_{TP}$
from below graph

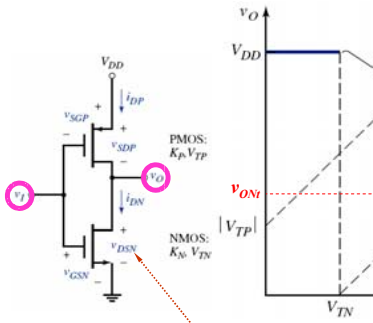
$V_{DD} - V_{OPt} = V_{DD} - V_{IPt} + V_{TP}$ or

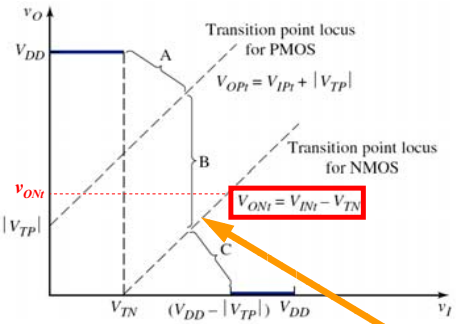
$V_{OPt} = V_{IPt} - V_{TP}$ V_{OPt} V_{IPt} PMOS output input voltage at the transition point.



V_{TP} is negative for an enhancement-mode PMOS

DC Analysis of the CMOS Inverter



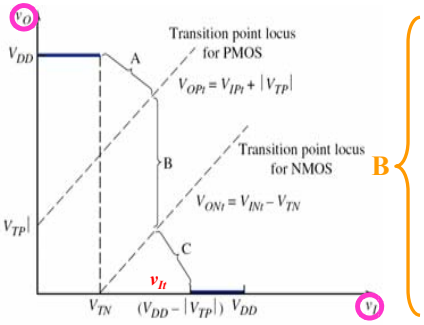


The transition point for the NMOS

$v_{DSN}(\text{sat}) = v_{GSN} - V_{TN}$
from above graph

$V_{ONt} = V_{INt} - V_{TN}$ V_{ONt} V_{INt} NMOS output input voltage at the transition point

DC Analysis of the CMOS Inverter



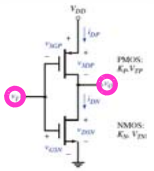
B when both transistors are in saturation
two drain currents equal

$$K_N(v_{GSN} - V_{TN})^2 = K_P(v_{SGP} + V_{TP})^2$$

$$K_N(v_I - V_{TN})^2 = K_P(V_{DD} - v_I + V_{TP})^2$$

$$v_I = v_{It} = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_N}{K_P}}V_{TN}}{1 + \sqrt{\frac{K_N}{K_P}}}$$

input voltage is a constant



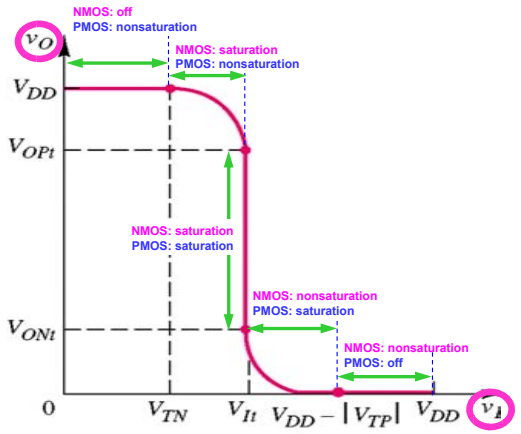
C For $v_I > V_{It}$, NMOS nonsaturation PMOS saturation
two drain currents equal

$$K_N[2(v_{GSN} - V_{TN})v_{DSN} - v_{DSN}^2] = K_P(v_{SGP} + V_{TP})^2$$

$$K_N[2(v_I - V_{TN})v_O - v_O^2] = K_P(V_{DD} - v_I + V_{TP})^2$$

DC Analysis of the CMOS Inverter

Complete voltage transfer characteristics



Example 16.9 p1041

Example 16.9 **Objective:** Determine the critical voltages on the voltage transfer curve of a CMOS inverter. v_{It} v_{OPt} v_{ONt}

Consider a CMOS inverter biased at $V_{DD} = 5\,\text{V}$ with transistor parameters of $K_N = K_P$ and $V_{TN} = -V_{TP} = 1\,\text{V}$. Then consider another CMOS inverter biased at $V_{DD} = 10\,\text{V}$ with the same transistor parameters.

For V_{DD}=5V

input voltage at the PMOS and NMOS transition points.

$$v_I = v_{It} = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_N}{K_P}}V_{TN}}{1 + \sqrt{\frac{K_N}{K_P}}} \qquad V_{It} = \frac{5 + (-1) + \sqrt{1}\cdot 1}{1 + \sqrt{1}} = 2.5\,\text{V}$$

output voltage at the transition point for the PMOS

$$V_{OPt} = V_{IPt} - V_{TP} \qquad V_{OPt} = V_{IPt} - V_{TP} = 2.5 - (-1) = 3.5\,\text{V}$$

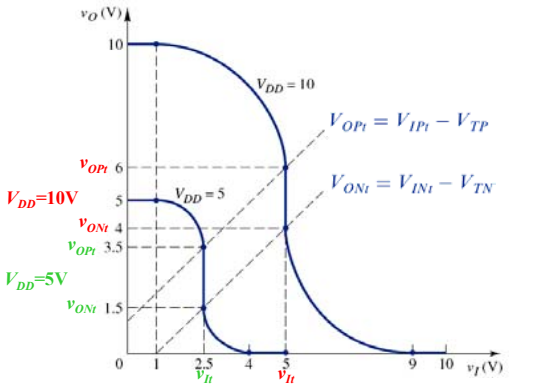
output voltage at the transition point for the NMOS

$$V_{ONt} = V_{INt} - V_{TN} \qquad V_{ONt} = V_{INt} - V_{TN} = 2.5 - 1 = 1.5\,\text{V}$$

For $V_{DD} = 10\,\text{V}$

$V_{It} = 5\,\text{V}$ $V_{OPt} = 6\,\text{V}$ $V_{ONt} = 4\,\text{V}$

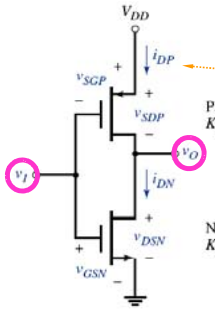
Example 16.9 p1041



Voltage transfer characteristics, CMOS inverter biased at either $V_{DD} = 5\,\text{V}$ or $V_{DD} = 10\,\text{V}$

DC Analysis of the CMOS Inverter

- CMOS inverter: series combination of PMOS and NMOS
- To form the input, gates of the two MOSFET are connected.
- To form the output, the drains are connected together.



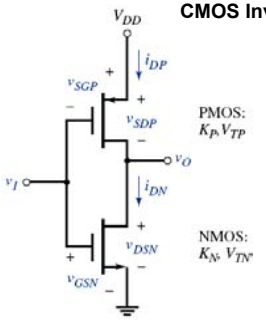
- The transistor K_N is also known as **"pull down"** device because it is pulling the output voltage down towards ground.
- The transistor K_P is known as the **"pull up"** device because it is pulling the output voltage up towards V_{DD}. This property speed up the operation considerably.

V_{In}	V_{Out}
1	0
0	1

The **static power dissipation** during both extreme cases (logic 1 or 0) is almost **zero** because $i_{DP} = i_{DN} = 0$.

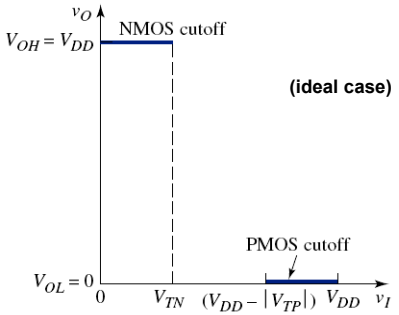
DC Analysis of the CMOS Inverter

CMOS Inverter in either High or Low State



Ideally, the power dissipation of the CMOS inverter is zero.

Practical device
CMOS inverter (~ nW)
NMOS inverter (~mW)



CMOS inverter output voltage for input voltage in either high state or low state

DC Analysis of the CMOS Inverter

Ideally, the current in the CMOS inverter in either steady-state condition is zero quiescent power dissipation is zero.

due to the reverse-biased pn junctions. the power dissipation may be in the nanowatt range rather than in the milliwatt range of NMOS inverters. Without this feature, VLSI would not be possible.

CMOS Inverter Design Consideration

❑ The CMOS inverter usually design to have,

(1) $$V_{TN} = |V_{TP}|$$

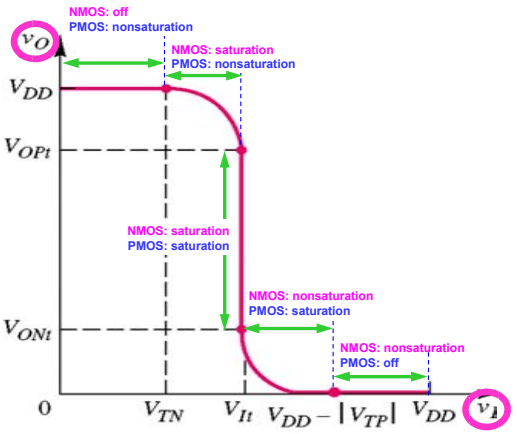
(2) $$k'_N\left(\frac{W}{L}\right) = k'_P\left(\frac{W}{L}\right)$$ But $k'_N > k'_P$ (because $\mu_N > \mu_P$)

➢ **How equation (2) can be satisfied ?**

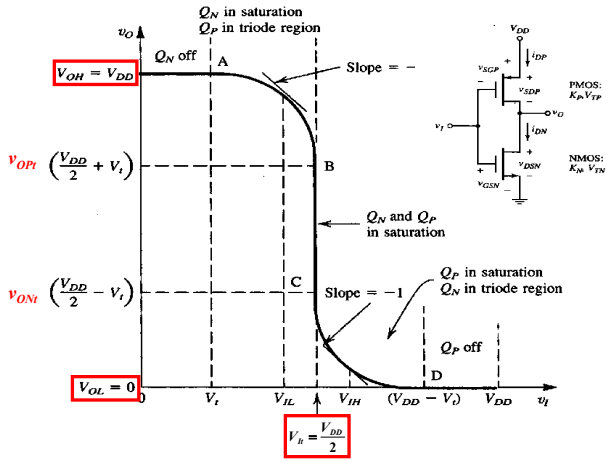
- ✓ This can achieved if **width of the PMOS** is made two or three times than that of the NMOS device.
- ✓ This is very important in order to provide a **symmetrical transition, results in wide noise margin.**

DC Analysis of the CMOS Inverter

Complete voltage transfer characteristics



Symmetrical Properties of the CMOS Inverter



The voltage transfer characteristic of the CMOS inverter.

p1101

For the CMOS inverter in Figure 16.34, let $V_{TN} = +0.4\,\text{V}$, $V_{TP} = -0.4\,\text{V}$, $k_n' = 80\,\mu\text{a/V}^2$, $k_p' = 40\,\mu\text{A/V}^2$, and $V_{DD} = 3.3\,\text{V}$. (a) Let $(W/L)_n = 2$ and $(W/L)_p = 4$. (i) Find the transition points for the p-channel and n-channel transistors. v_{It} v_{OPt} v_{ONt}
(ii) Find v_I when $v_O = 0.4\,\text{V}$ and when $v_O = 2.9\,\text{V}$.
(b) For $(W/L)_n = (W/L)_p = 2$, repeat part (a).

$$K_N = \frac{k_n'}{2}\left(\frac{W}{L}\right)$$

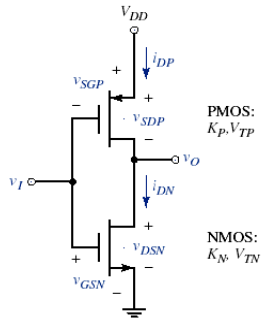


Figure 16.34 CMOS inverter

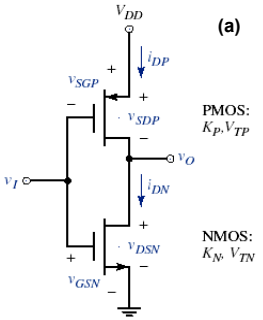


Figure 16.34 CMOS inverter

(a) $K_n = \left(\frac{80}{2}\right)(2) = 80\,\mu A/V^2$

$K_p = \left(\frac{40}{2}\right)(4) = 80\,\mu A/V^2$

(i) $V_{It} = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_n}{K_p}} \cdot V_{TN}}{1 + \sqrt{\frac{K_n}{K_p}}} = \frac{3.3 - 0.4 + (1)(0.4)}{1+1} = 1.65\,V$

Transition points

PMOS: $V_{OPt} = V_{It} - V_{TP} = 1.65 - (-0.4) \Rightarrow V_{OL} = 2.05\,V$

NMOS: $V_{ONt} = V_{It} - V_{TN} = 1.65 - (0.4) \Rightarrow V_{OL} = 1.25\,V$

(ii) For $v_O = 0.4\,V$: NMOS: Non-sat: PMOS:Sat

$K_n\left[2(V_{GSN} - V_{TN})V_{DS} - V_{DS}^2\right] = K_p\left[V_{SDP} + V_{TP}\right]^2$

$2(v_I - 0.4)(0.4) - (0.4)^2 = (3.3 - v_I - 0.4)^2$

$v_I = 1.89\,V$

For $v_O = 2.9\,V$, By symmetry

$v_I = 1.65 - (1.89 - 1.65) = 1.41\,V$

Example 16.29 p1101

(b) $K_n = \left(\frac{80}{2}\right)(2) = 80\ \mu A/V^2$

$K_p = \left(\frac{40}{2}\right)(2) = 40\ \mu A/V^2$

$$K_P = \frac{k_P'}{2}\left(\frac{W}{L}\right)$$

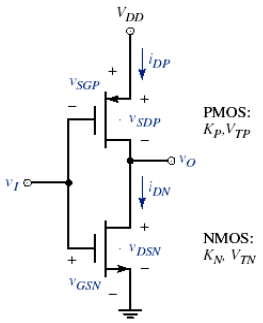


Figure 16.34 CMOS inverter

(i) $$V_{It} = \frac{3.3 - 0.4 + \sqrt{\frac{80}{40}}\cdot(0.4)}{1 + \sqrt{\frac{80}{40}}} = 1.44\ V$$

Transition points PMOS:
$V_{OPt} = 1.44 - (-0.4) \Rightarrow V_{Ot} = 1.84\ V$

NMOS:
$V_{ONt} = 1.44 - 0.4 \Rightarrow V_{Ot} = 1.04\ V$

(ii) For $v_o = 0.4\ V$

$(80)\left[2(v_I - 0.4)(0.4) - (0.4)^2\right] = (40)\left[3.3 - v_I - 0.4\right]^2$

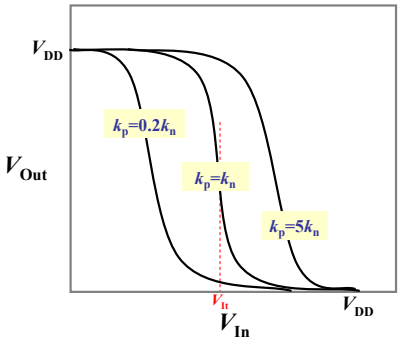
$v_I = 1.62\ V$

For $v_o = 2.9\ V$: NMOS:Sat, PMOS:Non-sat

$(80)\left[v_I - 0.4\right]^2 = (40)\left[2(3.3 - v_I - 0.4)(0.4) - (0.4)^2\right]$

$v_I = 1.16\ V$

CMOS Inverter V_{TC}



Increase W of PMOS
→ k_P increases
→ V_{It} moves to right

Increase W of NMOS
→ k_N increases
→ V_{It} moves to left

$$for \quad V_{It} = \frac{V_{DD}}{2}$$

$$\rightarrow \quad k_N = k_P\ ,\ W_N \approx W_P$$

$$v_I = v_{It} = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_N}{K_P}}V_{TN}}{1 + \sqrt{\frac{K_N}{K_P}}}$$

CMOS Inverter V_{TC}

Effects of V_{It} adjustment

- Result from changing k_P/k_N ratio:
  - Inverter threshold $V_{It} \neq V_{DD}/2$
  - Rise and fall delays unequal
  - Noise margins not equal
- Reasons for changing inverter threshold:
  - Want a faster delay for one type of transition (rise/fall)
  - Remove noise from input signal: increase one noise margin at expense of the other

Problem 16.31 p1101

16.31 Consider the series of CMOS inverters in Figure P16.31. The threshold voltages of the n-channel transistors are $V_{TN} = 0.8\,V$, and the threshold voltages of the p-channel transistors are $V_{TP} = -0.8\,V$. The conduction parameters are all equal. (a) Determine the range of v_{O1} for which both N_1 and P_1 are biased in the saturation region. (b) If $v_{O2} = 0.6\,V$, determine the values of v_{O3}, v_{O1}, and v_I.

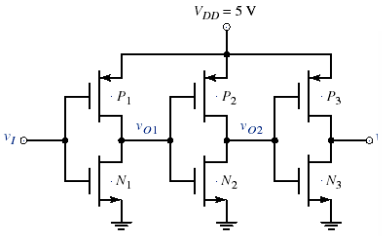


Figure P16.31

(a) $V_{ONt} \leq v_{O1} \leq V_{OPt}$

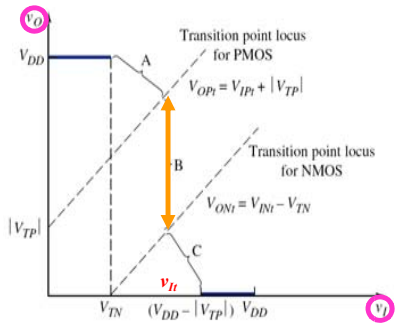
By symmetry, $V_{It} = 2.5\ V$

$V_{OPt} = 2.5 + 0.8 = 3.3\ V$

and $V_{ONt} = 2.5 - 0.8 = 1.7\ V$

So $1.7 \leq v_{O1} \leq 3.3\ V$

Problem 16.31 p1101



Example 16.31 p1101

16.31 Consider the series of CMOS inverters in Figure P16.31. The threshold voltages of the n-channel transistors are $V_{TN} = 0.8\,\text{V}$, and the threshold voltages of the p-channel transistors are $V_{TP} = -0.8\,\text{V}$. The conduction parameters are all equal. (a) Determine the range of v_{O1} for which both N_1 and P_1 are biased in the saturation region. (b) If $v_{O2} = 0.6\,\text{V}$, determine the values of v_{O3}, v_{O1}, and v_I.

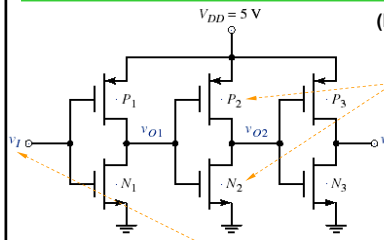


Figure P16.31

(b) For $v_{O2} = 0.6 < V_{TN} \Rightarrow v_{O3} = 5\,V$

N_2 in nonsaturation and P_2 in saturation. From Equation $K_N[2(v_I - V_{TN})v_O - v_O^2] = K_P(V_{DD} - v_I + V_{TP})^2$

$$[2(v_{I2} - 0.8)(0.6) - (0.6)^2] = [5 - v_{I2} - 0.8]^2$$

$$1.2v_{I2} - 1.32 = 17.64 - 8.4v_{I2} + v_{I2}^2$$

or

$$v_{I2}^2 - 9.6v_{I2} + 18.96 = 0$$

So $v_{I2} = v_{O1} = 2.78\,\text{V}$

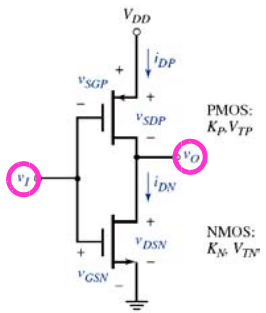
For $v_{O1} = 2.78$, both N_1 and P_1 in saturation. Then

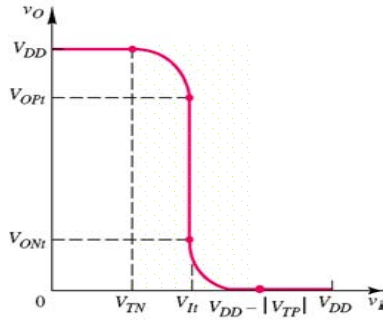
$v_I = 2.5\,\text{V}$

DC Analysis of the CMOS Inverter

CMOS inverter currents

- When the output of a CMOS inverter is either at a logic 1 or 0, the current in the circuit is zero.
- When the input voltage is in the range $V_{TN} < v_I < V_{DD} - |V_{TP}|$ both transistors are conducting and a current exists in the inverter.





DC Analysis of the CMOS Inverter

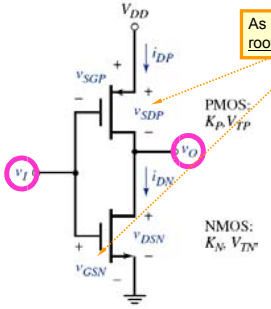
CMOS inverter currents

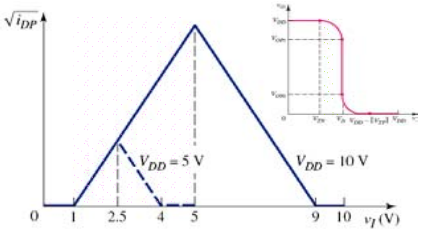
- **When NMOS transistor is biased in the saturation region**
  - The current in the inverter is controlled by v_{GSN} and the PMOS v_{SDP} adjusts such that $i_{DP} = i_{DN}$.

$$i_{DN} = i_{DP} = K_N(v_{GSN} - V_{TN})^2 = K_N(v_I - V_{TN})^2$$

$$\sqrt{i_{DN}} = \sqrt{i_{DP}} = \sqrt{K_N}(v_I - V_{TN})$$

As long as NMOS transistor is biased in the saturation region the square root of the inverter current is linear function of the input voltage.





Square root of inverter current versus input voltage, CMOS inverter biased at either $V_{DD} = 5\,\text{V}$ or $V_{DD} = 10\,\text{V}$

DC Analysis of the CMOS Inverter

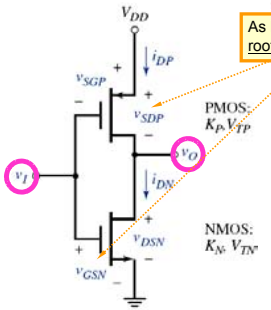
CMOS inverter currents

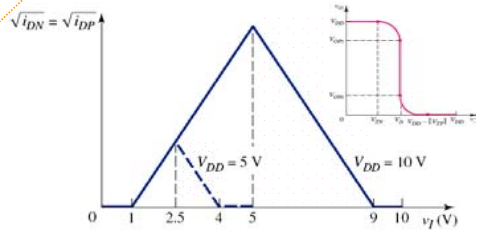
- **When PMOS transistor is biased in the saturation region**
  - The current in the inverter is controlled by v_{SGP} and the NMOS v_{DSN} adjusts such that $i_{DP} = i_{DN}$.

$$i_{DN} = i_{DP} = K_P(V_{DD} - v_I + V_{TP})^2$$

$$\sqrt{i_{DN}} = \sqrt{i_{DP}} = \sqrt{K_P}(V_{DD} - v_I + V_{TP})$$

As long as PMOS transistor is biased in the saturation region the square root of the inverter current is linear function of the input voltage.





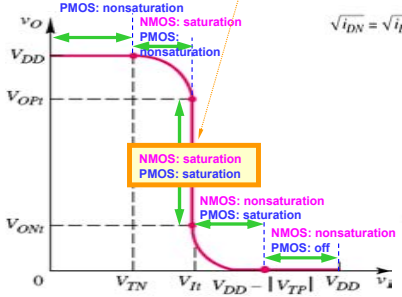
Square root of inverter current versus input voltage, CMOS inverter biased at either $V_{DD} = 5$ V or $V_{DD} = 10$ V

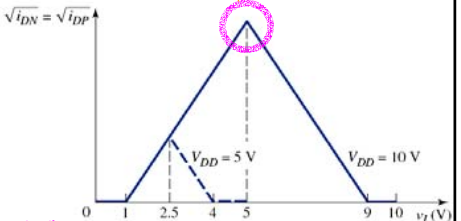
DC Analysis of the CMOS Inverter

CMOS inverter currents

At the inverter switching point, both transistors are biased in the saturation region and both transistors influence the current.

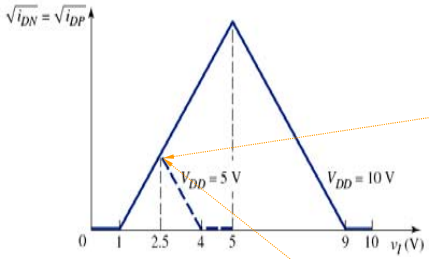
→ the actual current characteristic does not have a sharp discontinuity in the slope.





Problem 16.33 p1102

16.33 The transistor parameters in the CMOS inverter are: $k_n' = 50\,\mu A/V^2$, $k_p' = 25\,\mu A/V^2$, $V_{TN} = 0.8$ V, and $V_{TP} = -0.8$ V. (a) For $(W/L)_n = 2$ and $(W/L)_p = 4$, determine the peak current in the inverter during a switching cycle for $V_{DD} = 5$ V. (b) Repeat part (a) for $(W/L)_n = (W/L)_p = 2$.



(a) $K_n = \left(\frac{50}{2}\right)(2) = 50\ \mu A/V^2$

$K_p = \left(\frac{25}{2}\right)(4) = 50\ \mu A/V^2$

$I_{D,peak} = K_n(v_I - V_{TN})^2 = 50(2.5 - 0.8)^2$

or $I_{D,peak} = 144.5\ \mu A$

(b) $K_n = 50\ \mu A/V^2$, $K_p = 25\ \mu A/V^2$

From Equation (16.55),

$$V_{It} = \frac{5 - 0.8 + \sqrt{\frac{50}{25}}(0.8)}{1 + \sqrt{\frac{50}{25}}} = 2.21\,V$$

Then

$I_{D,peak} = K_n(V_{It} - V_{TN})^2 = 50(2.21 - 0.8)^2$

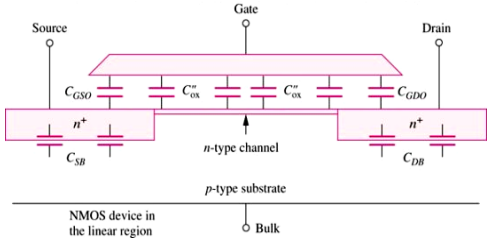
or $I_{D,peak} = 99.4\ \mu A$

Power Dissipation

- There is **no power dissipation in the CMOS inverter** when the output is either at logic 0 or 1. However, during **switching** of the CMOS inverter from low logic 0 to logic 1, current flows and power is dissipated.
- Usually CMOS inverter and logic circuit are used to drive other MOS devices by connecting a capacitor across the output of a CMOS inverter. This **capacitor** must be charged and discharged during the switching cycle.

NMOS Transistor Capacitances

Triode Region



C_{ox}" = Gate-Channel capacitance per unit area(F/m^2)

C_{GC} = Total gate channel capacitance

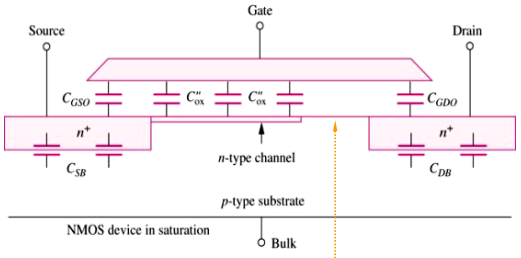
C_{GS} = Gate-Source capacitance

C_{GD} = Gate-Drain capacitance

C_{GSO} and C_{GDO} = overlap capacitances (F/m)

NMOS Transistor Capacitances

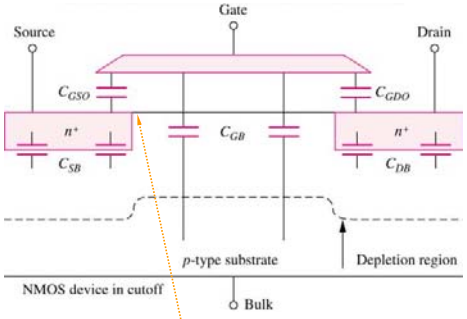
Saturation Region



- Drain is no longer connected to channel.

NMOS Transistor Capacitances

Cutoff Region



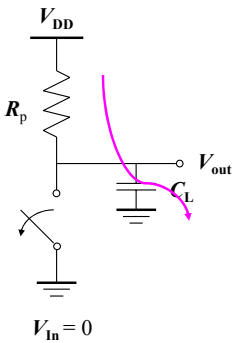
- Conducting channel region is completely gone.

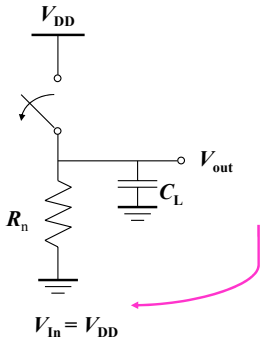
C_{GB} = Gate-Bulk capacitance

C_{GBO} = Gate-Bulk capacitance per unit width.

CMOS Inverter

Switch Model of Dynamic Behavior





- Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

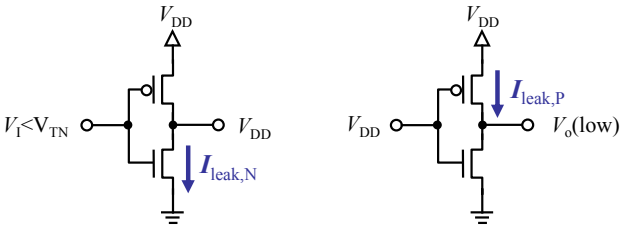
CMOS Inverter Power

- Power has three components
  - **Static power**: when input isn't switching
  - **Dynamic capacitive power**: due to charging and discharging of load capacitance
  - **Dynamic short-circuit power**: direct current from V_{DD} to G_{nd} when both transistors are on

CMOS Inverter Power

Static Power Consumption

- Static current: in CMOS there is no static current as long as $V_{In} < V_{TN}$ or $V_{In} > V_{DD}+V_{TP}$
- Leakage current: determined by "off" transistor
- Influenced by transistor width, supply voltage, transistor threshold voltages



CMOS Inverter Power

Dynamic Capacitive Power and Energy stored in the PMOS

Case I: When the input is at logic 0

PMOS is conducting and NMOS is in cutoff mode and the load capacitor must be charged through the PMOS device.

Power dissipation in the PMOS transistor;

$P_P=i_L V_{SDp}= i_L(V_{DD}-V_O)$

The current and output voltages are related by,

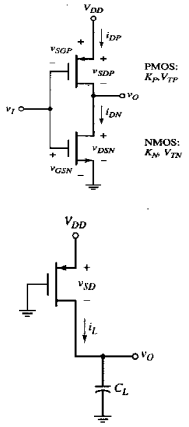
$i_L=C_L dv_O/dt$

Similarly the **energy dissipation** in the PMOS device

$$E_P = \int_0^{\infty} P_P = \int_0^{\infty} C_L(V_{DD}-v_O)\frac{dv_O}{dt}\,dt, E_P = C_L V_{DD}\int_0^{V_{DD}} dv_O - C_L\int_0^{V_{DD}} v_O dv_O$$

$$E_P = C_L V_{DD} v_O\Big|_0^{V_{DD}} - C_L\frac{v_O^2}{2}\Big|_0^{V_{DD}}, E_P = (C_L V_{DD}V_{DD}-0)-(C_L\frac{V_{DD}^2}{2}-0)$$

$E_P = \frac{1}{2}C_L V_{DD}^2$ the energy stored in the capacitor CL when the output is high.



CMOS Inverter Power

Dynamic Capacitive Power and Energy stored in the PMOS

Case II: when the input is high and out put is low:

During switching all the energy stored in the load capacitor is dissipated in the NMOS device because NMOS is conducting and PMOS is in cutoff mode.

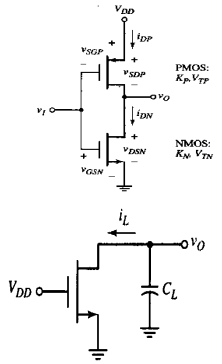
The energy dissipated in the NMOS inverter;

$E_N = \frac{1}{2}C_L V_{DD}^2$

The total energy dissipated during one switching cycle $E_T = E_P + E_N = \frac{1}{2}C_L V_{DD}^2 + \frac{1}{2}C_L V_{DD}^2 = C_L V_{DD}^2$

The $E_T = P \cdot t \rightarrow P = \frac{E_T}{t} \rightarrow P = fE_T \rightarrow fC_L V_{DD}^2$

This implied that the **power dissipation** in the CMOS inverter is directly proportional to switching frequency and V_{DD}^2



CMOS Inverter Power

Dynamic Capacitive Power

$$P_{dyn} = C_L V_{DD}^2 f$$

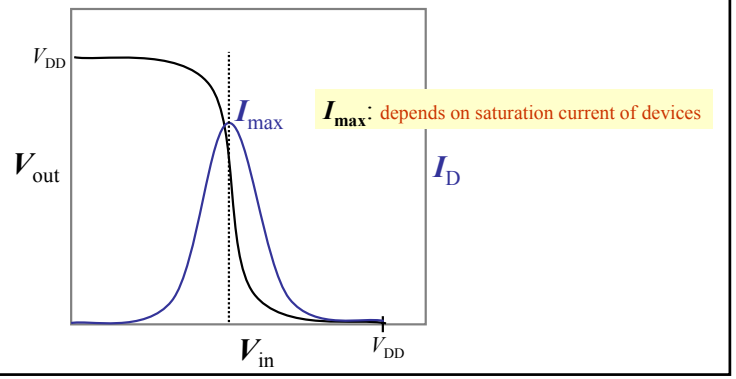
Formula for dynamic power

- Does not (directly) depend on device sizes
- Does not depend on switching delay
- Applies to general CMOS gate in which:
  - Switched capacitances are lumped into C_L
  - Output swings from GND to V_{DD}
  - Input signal approximated as step function
  - Gate switches with frequency f

CMOS Inverter Power

Dynamic Short-Circuit Power

- Short-circuit current flows from V_{DD} to GND when both transistors are on saturation mode.



Inverter Power Consumption

Total Power Consumption

$$P_{tot} = P_{dyn} + P_{sc} + P_{stat}$$

$$P_{tot} = C_L V_{DD}^2 f + V_{DD} I_{max} \left(\frac{t_r + t_f}{2} \right) f + V_{DD} I_{leak}$$

$$P_{tot} \sim C_L V_{DD}^2 f$$

Power Reduction

- **Reducing dynamic capacitive power**
  - **Lower the voltage!!**
    - Quadratic effect on dynamic power
  - **Reduce capacitance!!**
    - Short interconnect lengths
    - Drive small gate load (small gates, small fan-out)
  - **Reduce frequency!!** $P_{dyn} = C_L V_{DD}^2 f$
    - Lower clock frequency
    - Lower signal activity

Power Reduction

- **Reducing short-circuit current**
  - Fast rise/fall times on input signal
  - Reduce input capacitance
  - Insert small buffers to "clean up" slow input signals before sending to large gate
- **Reducing leakage current**
  - Small transistors (leakage proportional to width)
  - Lower voltage

Example 16.10 on Page 1045

Given that for a CMOS inverter

$C_L = 2\,pF$

$V_{DD} = 5V$

$f = 100\,KHz$

Calculate the power dissipation in the CMOS inverter

Sol:

As we know relation between power, frequency and capacitance

$$P = f C_L V_{DD}^2$$

$$\Rightarrow P = (10^5)(2 \times 10^{-12})(5)^2$$

$$P = 5 \times 10^{-6} W$$

Comments:

The typical values of static power dissipation in NMOS inverter is on the order of 500MW. The power dissipation of the CMOS inverter in the above example is 5MW which is 100 time smaller than NMOS inverter.

$\Rightarrow$ CMOS is ideal for practide applications (Integrated digital circuits.

The power dissipation can

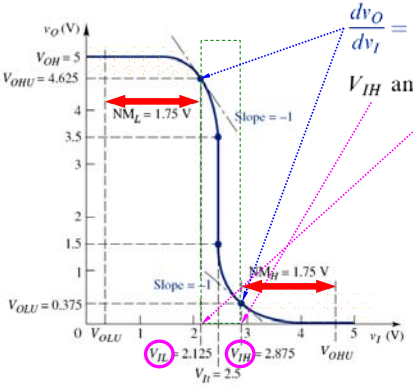
Chapter 16

MOSFET Digital Circuits

Chapter 16.3.4

CMOS Inverter Noise Margin

Concept of Noise Margins



CMOS inverter voltage transfer characteristics with defined noise margins

$$\frac{dv_O}{dv_I} = -1$$

V_{IH} and V_{IL} determine the noise margins

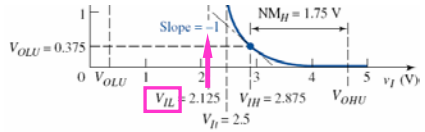
For $V_{IL} < v_I < V_{IH}$,
the inverter gain is greater than unity, and the output signal changes rapidly with input voltage.

For $v_I \le V_{IL}$ and $v_I \ge V_{IH}$,
the inverter gain is less than unity and the output changes slowly with input voltage.

$NM_L = V_{IL} - V_{OLU}$ Noise Margin for low input

$NM_H = V_{OHU} - V_{IH}$ Noise Margin for high input

CMOS Inverter Noise Margins



Point V_{IL} NMOS is saturation PMOS is nonsaturation

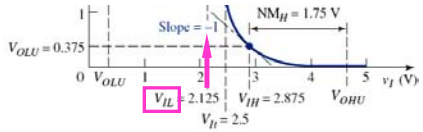
The relationship between the input and output voltages of CMOS when NMOS is saturation PMOS is nonsaturation

$$i_{DN} = i_{DP}$$

$$K_N[v_{GSN} - V_{TN}]^2 = K_P[2(v_{SGP} + V_{TP})v_{SDP} - v_{SDP}^2]$$

$$K_N[v_I - V_{TN}]^2 = K_P[2(V_{DD} - v_I + V_{TP})(V_{DD} - v_O) - (V_{DD} - v_O)^2]$$

CMOS Inverter Noise Margins



Point V_{IL} NMOS is saturation PMOS is nonsaturation

The relationship between the input and output voltages of CMOS when NMOS is saturation PMOS is nonsaturation

$$K_N[v_I - V_{TN}]^2 = K_P[2(V_{DD} - v_I + V_{TP})(V_{DD} - v_O) - (V_{DD} - v_O)^2]$$

Taking the derivative with respect to v_I

$$2K_N[v_I - V_{TN}] = K_P\left[-2(V_{DD} - v_O) - 2(V_{DD} - v_I + V_{TP})\frac{dv_O}{dv_I} - 2(V_{DD} - v_O)\left(-\frac{dv_O}{dv_I}\right)\right]$$

$\frac{dv_O}{dv_I} = -1$ →

$$K_N[v_I - V_{TN}] = -K_P[(V_{DD} - v_O) - (V_{DD} - v_I + V_{TP}) + (V_{DD} - v_O)]$$

$$v_O = V_{OHU} = \frac{1}{2}\left\{\left(1 + \frac{K_N}{K_P}\right)v_I + V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}\right\}$$

$$v_I = V_{IL} = V_{TN} + \frac{(V_{DD} + V_{TP} - V_{TN}}{\left(\frac{K_N}{K_P} - 1\right)}\left[2\sqrt{\frac{\frac{K_N}{K_P}}{\frac{K_N}{K_P} + 3}} - 1\right]$$

CMOS Inverter Noise Margins

$$v_O = V_{OHU} = \frac{1}{2}\left\{\left(1 + \frac{K_N}{K_P}\right)v_I + V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}\right\}$$

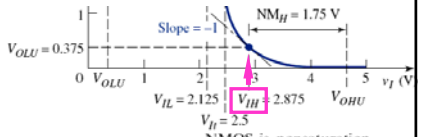
If CMOS is symmetrical, $K_N = K_P$

$$v_O = V_{OHU(K_N=K_P)} = \tfrac{1}{2}\{2v_I + V_{DD} - V_{TN} - V_{TP}\}$$

$$K_N[v_I - V_{TN}]^2 = K_P[2(V_{DD} - v_I + V_{TP})(V_{DD} - v_O) - (V_{DD} - v_O)^2]$$

$$v_I = V_{IL(K_N=K_P)} = V_{TN} + \tfrac{3}{8}(V_{DD} + V_{TP} - V_{TN}) \quad \text{for } K_N = K_P$$

CMOS Inverter Noise Margins



Point V_{IH}

The relationship between the input and output voltages of CMOS when NMOS is nonsaturation PMOS is saturation

$$K_N[2(v_I - V_{TN})v_O - v_O^2] = K_P(V_{DD} - v_I + V_{TP})^2$$

Taking the derivative with respect to v_I

$$K_N\left[2(v_I - V_{TN})\frac{dv_O}{dv_I} + 2v_O - 2v_O\frac{dv_O}{dv_I}\right] = 2K_P(V_{DD} - v_I + V_{TP})(-1)$$

$\frac{dv_O}{dv_I} = -1$ →

$$K_N[-(v_I - V_{TN}) + v_O + v_O] = -K_P[V_{DD} - v_I + V_{TP}]$$

$$v_O = V_{OLU} = \frac{v_I\left(1 + \frac{K_N}{K_P}\right) - V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}}{2\left(\frac{K_N}{K_P}\right)}$$

$$v_I = V_{IH} = V_{TN} + \frac{(V_{DD} + V_{TP} - V_{TN})}{\left(\frac{K_N}{K_P} - 1\right)}\left[\frac{2\frac{K_N}{K_P}}{\sqrt{3\frac{K_N}{K_P} + 1}} - 1\right]$$

CMOS Inverter Noise Margins

$$v_O = V_{OLU} = \frac{v_I\left(1+\frac{K_N}{K_P}\right) - V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}}{2\left(\frac{K_N}{K_P}\right)}$$

If CMOS is symmetrical, $K_N = K_P$

$$v_O = V_{OLU(K_N=K_P)} = \tfrac{1}{2}\{2v_I - V_{DD} - V_{TN} - V_{TP}\}$$

$$K_N[2(v_I - V_{TN})v_O - v_O^2] = K_P(V_{DD} - v_I + V_{TP})^2$$

$$v_I = V_{IH(K_N=K_P)} = V_{TN} + \tfrac{5}{8}(V_{DD} + V_{TP} - V_{TN}) \quad \text{for } K_N = K_P$$

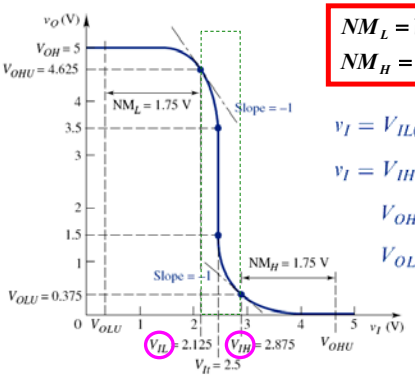
CMOS Inverter Noise Margins

Summary

Noise Margin of a Symmetrical CMOS Inverter

$NM_L = V_{IL} - V_{OLU}$ Noise Margin for low input

$NM_H = V_{OHU} - V_{IH}$ Noise Margin for high input



CMOS inverter voltage transfer characteristics with defined noise margins

$$v_I = V_{IL(K_N=K_P)} = V_{TN} + \tfrac{3}{8}(V_{DD} + V_{TP} - V_{TN})$$

$$v_I = V_{IH(K_N=K_P)} = V_{TN} + \tfrac{5}{8}(V_{DD} + V_{TP} - V_{TN})$$

$$V_{OHU(K_N=K_P)} = \tfrac{1}{2}\{2v_I + V_{DD} - V_{TN} - V_{TP}\}$$

$$V_{OLU(K_N=K_P)} = \tfrac{1}{2}\{2v_I - V_{DD} - V_{TN} - V_{TP}\}$$

Example 16.11 P1047

Example 16.11 **Objective:** Determine the noise margins of a CMOS inverter.

Consider a CMOS inverter biased at $V_{DD} = 5$ V. Assume the transistors are matched with $K_N = K_P$ and $V_{TN} = -V_{TP} = 1$ V.

$$v_I = V_{IL(K_N=K_P)} = V_{TN} + \tfrac{3}{8}(V_{DD} + V_{TP} - V_{TN})$$

$$V_{IL} = V_{TN} + \tfrac{3}{8}(V_{DD} + V_{TP} - V_{TN}) = 1 + \tfrac{3}{8}(5 - 1 - 1) = 2.125 \text{ V}$$

$$v_I = V_{IH(K_N=K_P)} = V_{TN} + \tfrac{5}{8}(V_{DD} + V_{TP} - V_{TN})$$

$$V_{IH} = V_{TN} + \tfrac{5}{8}(V_{DD} + V_{TP} - V_{TN}) = 1 + \tfrac{5}{8}(5 - 1 - 1) = 2.875 \text{ V}$$

$$V_{OHU(K_N=K_P)} = \tfrac{1}{2}\{2v_I + V_{DD} - V_{TN} - V_{TP}\} \qquad V_{OLU(K_N=K_P)} = \tfrac{1}{2}\{2v_I - V_{DD} - V_{TN} - V_{TP}\}$$

$$V_{OHU} = \tfrac{1}{2}[2V_{IL} + V_{DD} - V_{TN} - V_{TP}] = \tfrac{1}{2}[2(2.125) + 5 - 1 + 1] = 4.625 \text{ V}$$

$$V_{OLU} = \tfrac{1}{2}[2V_{IH} - V_{DD} - V_{TN} - V_{TP}] = \tfrac{1}{2}[2(2.875) - 5 - 1 + 1] = 0.375 \text{ V}$$

noise margins

$$NM_H = V_{OHU} - V_{IH} = 4.625 - 2.875 = 1.75 \text{ V} \qquad NM_L = V_{IL} - V_{OLU} = 2.125 - 0.375 = 1.75 \text{ V}$$

Chapter 16

MOSFET Digital Circuits

Chapter 16.4

CMOS Logic Circuits

CMOS Logic Circuits

- Large scale integrated CMOS logic circuits including watches, calculators, and microprocessors are constructed by using basic CMOS NOR and NAND gates.

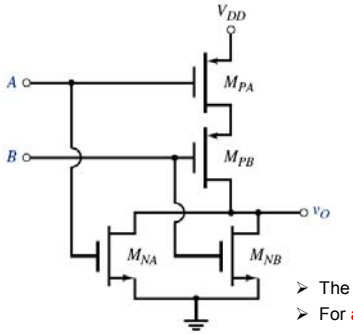
  Therefore, understanding of these basic gates is very important for the designing of very large scale integrated (VLSI) logic circuits.

CMOS NOR and NAND Gates

CMOS Logic Circuits

CMOS NOR and NAND Gates

- CMOS **NOR gate** can be constructed by using **two parallel NMOS** devices and **two series PMOS** transistors.



Two-input CMOS NOR logic circuit

truth table

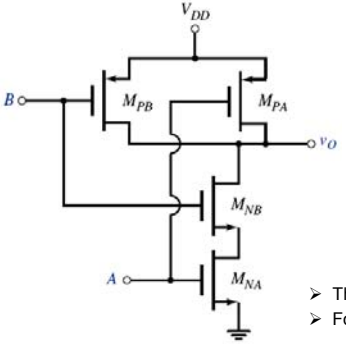
A	B	v_O
0	0	V_{DD}
V_{DD}	0	0
0	V_{DD}	0
V_{DD}	V_{DD}	0

- The output is at **logic 1** when **all inputs are low**.
- For **all other** possible inputs, output is low or at **logic 0**.

CMOS Logic Circuits

CMOS NOR and NAND Gates

- CMOS **NAND gate** can be constructed by using **two parallel PMOS** devices and **two series NMOS** transistors.



Two-input CMOS NAND logic circuit

truth table

A	B	v_O
0	0	V_{DD}
V_{DD}	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

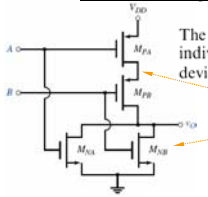
- The is at **logic 0** when **all inputs are high**.
- For **all other** possible inputs, output is high or at **logic 1**.

CMOS Logic Circuits

How can we design CMOS NOR symmetrical gate?

To obtained symmetrical switching times for the high-to-low and low-to-high output transitions, the effective conduction (design) parameters of the **composite** PMOS and **composite** NMOS device must be equal.

For the CMOS NOR gate, $K_{CN} = K_{CP}$ effective conduction parameter of the two parallel NMOS / two series PMOS



The effective channel *width* of the parallel NMOS devices is twice the individual width; similarly, the effective channel *length* of the series PMOS devices is twice the individual length.

$$\frac{k_n'}{2}\left(\frac{2W}{L}\right)_N = \frac{k_p'}{2}\left(\frac{W}{2L}\right)_P$$

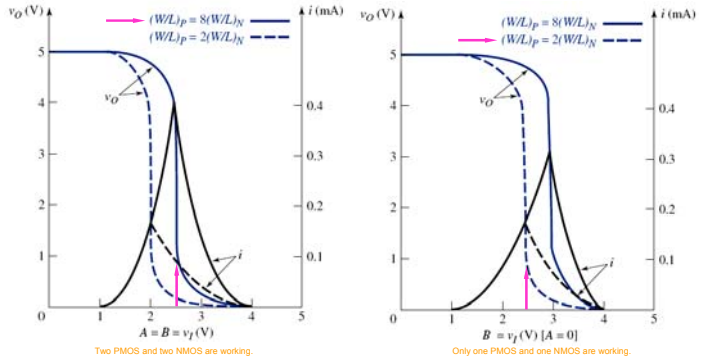
$$k_n' \approx 2k_p' \Rightarrow 2\left(\frac{2W}{L}\right)_N = \left(\frac{W}{2L}\right)_P \Rightarrow \left(\frac{W}{L}\right)_P = 8\left(\frac{W}{L}\right)_N$$

In order to get the symmetrical switching properties, the width to length ratio of **PMOS** transistor must be approximately eight times that of the NMOS device.

For asymmetrical case, switching time is longer!!

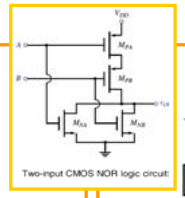
CMOS Logic Circuits

How can we design CMOS NOR symmetrical gate?

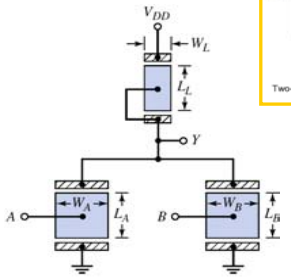


Voltage transfer characteristics, two-input CMOS NOR logic circuit for various width-to-length ratios

Concept of Effective Width to Length Ratios

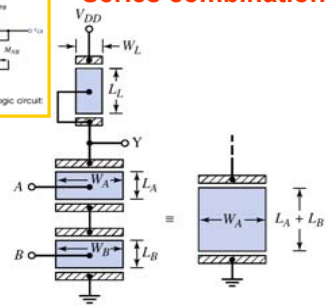


Parallel combination



For the **NOR gate** the **effective width of the drivers transistors doubles.**
The effective aspect ratio is increased.

Series combination



For the **NAND gate** the **effective length of the driver transistors doubles.**
The effective aspect ratio is decreased.

D16.19 In the two-input CMOS NAND gate in Figure 16.45(a), determine the relationship between the (W/L) ratios of the n-channel and p-channel transistors such that the composite conduction parameters of the PMOS and NMOS devices are equal. (Ans. $(W/L)_N = 2(W/L)_P$)

D16.20 Design a three-input CMOS NOR logic gate such that the effective conduction parameters of the composite PMOS and NMOS transistors are equal. Determine $(W/L)_P/(W/L)_N$, where (W/L) is the width-to-length ratio of the individual PMOS and NMOS transistors. (Ans. $(W/L)_P = 18(W/L)_N$)

D16.19 on page 1051

Reference: 2-input CMOS NAND gate.

Determine relationship b/w the n-channel and p-channel transistors, such that composite conduction parameters of the PMOS and NMOS devices are equal. i.e $K_{N,eff} = K_{P,eff}$

Sol: Inspection of figure 16.45a shows that the effective channel width of the parallel p MOS device is twice the individual width and effective channel length of the series NMOS transistors is twice the individual length i.e.

$$\left(\frac{K_N'}{2}\right)\left(\frac{W}{2L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{2W}{L}\right)_P$$

Since $K_N' \simeq 2K_P'$

$$\Rightarrow \left(\frac{2K_P'}{2}\right)\left(\frac{W}{2L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{2W}{L}\right)_P$$

$$\Rightarrow \frac{1}{2}\left(\frac{W}{L}\right)_N = K_P'\left(\frac{W}{L}\right)_P$$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_P}$$

16.20 on page 1051

Design a three input CMOS NOR logic gate such that $K_{N,eff} = K_{P,eff}$

Determine $\left(\frac{W}{L}\right)_P / \left(\frac{W}{L}\right)_N$

Sol: In case of the input CMOS NOR gate we have three NMOS parallel transistors three PMOS series transistor

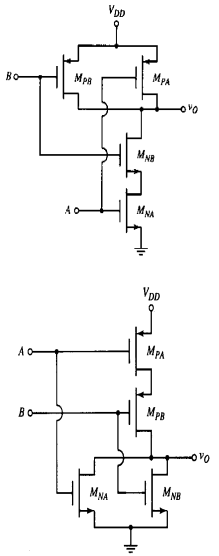
$$\Rightarrow \left(\frac{K_N'}{2}\right)\left(\frac{3W}{L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{}{}\right)$$

Since $K_N' \simeq 2K_P'$

$$\left(\frac{2K_P'}{2}\right)\left(\frac{3W}{L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{}{}\right)$$

$$3\left(\frac{W}{L}\right)_N = \frac{1}{6}\left(\frac{W}{L}\right)_P$$

$$\Rightarrow \boxed{\frac{\left(\frac{W}{L}\right)_P}{\left(\frac{W}{L}\right)_N} = 18}$$



CMOS Logic Circuits

Fan-In and Fan-Out

- **Fan-in** of a gate is the **number of its inputs**.
  Thus a four input NOR gate has a fan-In of 4.
- **Fan-Out** is the **maximum number of load gates** that may be connected to the output.

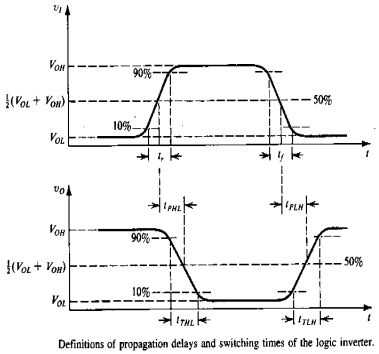
Since the CMOS logic gate will be driving other CMOS logic gates, the quiescent currrent required to drive the other CMOS gates is essentially zero. ➡ the maximum fanout is virtually limitless.

However,

- Each additional load gate increases the load capacitance their must be charge and discharge as the driver gate changes state. This place a **practical limit on the maximum allowable number of load gates**.

Switching Time and Propagation Delay Time

- The dynamic performance of a logic circuit family is characterized by propagation delay of its basic inverter. The propagation delay time is define as the *average of low-to-high propagation delay time and the high-to-low propagation delay time.*
- The propagation delay time is directly proportional to the **switching time** and increases as the Fan-out increases. Therefore, the maximum Fan-out is limited by the maximum acceptable propagation delay time.



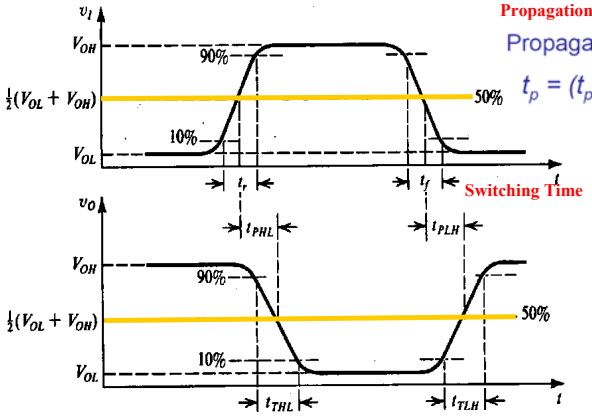
Definitions of propagation delays and switching times of the logic inverter.

Each additional load gate increases the load capacitance their must be charge and discharge as the driver gate changes state. This place a practical limit on the maximum allowable number of load gates.

CMOS Logic Circuits

Switching Time and Propagation Delay Time

Definitions of propagation delays and switching times of the logic inverter.



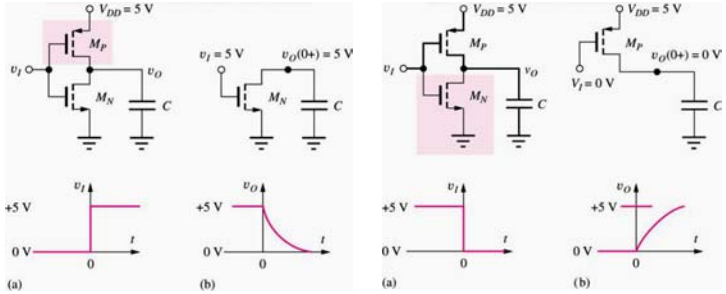
Propagation Delay Time

Propagation delay

$t_p = (t_{pHL} + t_{pLH})/2$

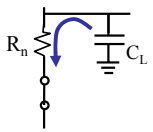
Switching Time

Propagation Delay Estimate



- The two modes of capacitive charging/discharging that contribute to propagation delay

Switch-level model



Delay estimation using switch-level model (for general RC circuit):

$$I = C\frac{dV}{dt} \quad \rightarrow \quad dt = \frac{C}{I}dV$$

$$I = \frac{V}{R} \quad \rightarrow \quad dt = \frac{RC}{V}dV$$

$$t_1 - t_0 = t_p = \int_{V_0}^{V_1} \frac{RC}{V}dV$$

$$t_p = RC\left[\ln(V_1) - \ln(V_0)\right] = RC\ln\left(\frac{V_1}{V_0}\right)$$

Switch-level model

- For fall delay t_{phl}, $V_0=V_{cc}$, $V_1=V_{cc}/2$

$$t_p = RC\ln\left(\frac{V_1}{V_0}\right) = RC\ln\left(\frac{\frac{1}{2}V_{CC}}{V_{CC}}\right)$$

$$t_p = RC\ln(0.5)$$

$$t_{phl} = 0.69R_nC_L$$

$$t_{plh} = 0.69R_pC_L$$

← Standard RC-delay equations

Chapter 16

MOSFET Digital Circuits

Chapter 16.6

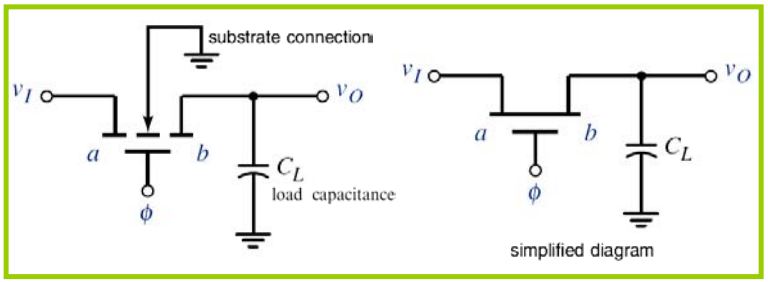
Transmission Gates

Transmission Gates

- Use of transistors as **switches** between driving circuits and load circuits are called **transmission gates** because switches can transmit information from one circuit to another.
- NMOS and CMOS transmission gate.

NMOS Transmission Gate

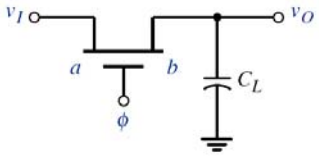
- **The bias applied to the transistor determines** which terminal acts as the ***drain*** and which terminal acts as the ***source***.



- C_L load capacitance input gate capacitance of a MOS logic circuit.
- transistor must be bilateral
  must be able to conduct current in either direction.
  This is a natural feature of MOSFETs.

NMOS Transmission Gate

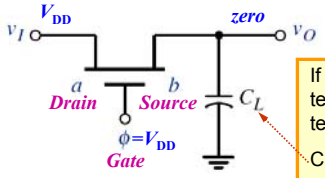
As an Open Switch



When gate voltage ϕ=0, the n-channel transistor is **cut-off** and the transistor acts as an ***open switch***

NMOS Transmission Gate

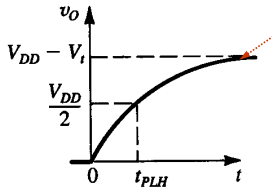
As an Open Switch



@ High input

If $\phi=V_{DD}$, $v_I=V_{DD}$, and v_O is initially (t=0) *zero*, terminal *a* acts as the **drain** since its bias is V_{DD}. terminal *b* acts as the **source** since its bias is *zero*.

Current enters the drain from the input charging up the **capacitor**.

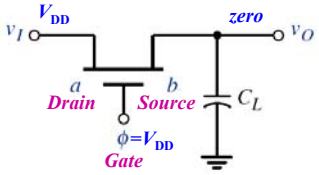


As CL charges up and Vo increases, the gate to source voltage decreases. When the gate to source voltage VGS become equal to threshold voltage VTN, the capacitance stop charging and current goes to zero.
This implies that the
VO=VO(max) when VGS=VTN
Or
VO(max) = V_{DD}-VTN

This implies that output voltage never will be equal to V_{DD}. ; rather it will be lower by V_{TN}.
This is one of the disadvantage of an NMOS transmission gate when VI=high

NMOS Transmission Gate

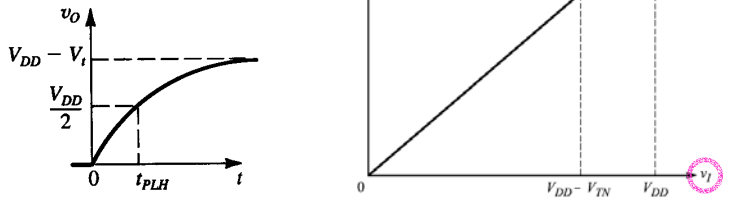
As an Open Switch



@ High input

$v_{GS} = \phi - v_O = V_{DD} - v_O$

$v_O(\max) = V_{DD} - V_{TN}$



Output voltage versus input voltage characteristics

Characteristics of NMOS transmission gate (at low input)

- When V_I=0 and ϕ=V_{DD}

and V_O=V_{DD}-V_{TN} at t=o (initially).

It is to be noted that in the present case terminal b acts as the drain and terminal a acts as the source.

Under these conditions the gate to source voltage is,

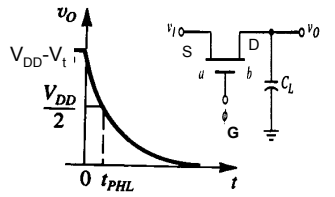
$$V_{GS}=\phi-V_I$$
$$V_{GS}=V_{DD}-o$$
$$V_{GS}=V_{DD}$$

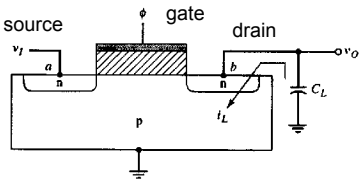
This implies that value of V_{GS} is constant.

In this case the capacitor is fully discharge to zero as the drain current goes to zero.

$$V_O=0$$

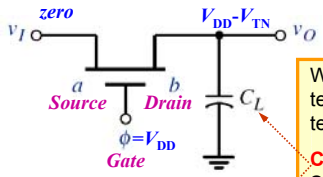
This implies that the NMOS transistor provide a "good" logic 0 when V_I=low





NMOS Transmission Gate

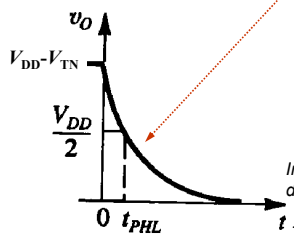
As an Open Switch



@ Low input

When ϕ=V_{DD}, v_I=0, and v_O=V_{DD}-V_{TN}, at t=0, terminal *a* acts as the **source** since its bias is *zero*. terminal *b* acts as the **drain** since its bias is *high*.

Capacitor discharges as current enters the drain. Stop discharging drain current goes *zero*.



$$v_{GS}=\phi-v_I=V_{DD}-0=V_{DD}$$

v_{GS} is a constant

"Good" logic 0 when V_I=low

In this case the capacitor is fully discharge to zero as the drain current goes to zero.

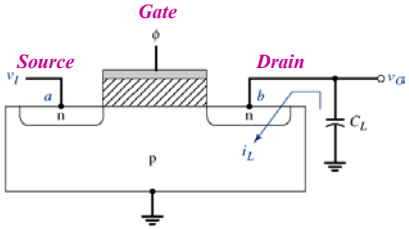
V_O=0

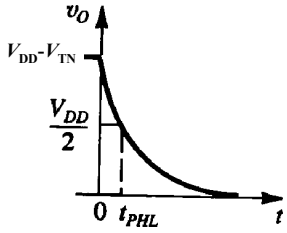
This implies that the NMOS transistor provide a "good" logic 0 when VI=low

NMOS Transmission Gate

- Why NMOS transmission gate does **not** remain in a **static condition**?

  - The **reverse leakage current** due to reverse bias between terminal *b* and ground begins to **discharge the capacitor**, and the circuit does not remain in a static condition.

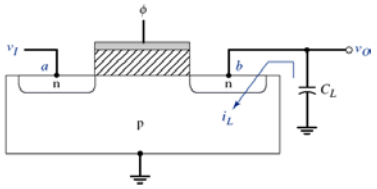




Example 16.13 p1060

Example 16.13 **Objective:** Estimate the rate at which the output voltage v_O in Figure 16.57 decreases with time.

Assume the capacitor is initially charged to $v_O = 4$ V. Let $C_L = 1$ pF and assume the reverse-biased pn junction leakage current is a constant at $i_L = 1$ nA.



The voltage across the capacitor

$$v_O = -\frac{1}{C_L}\int i_L dt = -\frac{i_L}{C_L}t + K_1$$

minus sign indicates that the current is leaving the positive terminal of the capacitor.

$$K_1 = v_O(t=0) = 4\text{ V} \quad \text{initial condition}$$

$$v_O = 4 - \frac{i_L}{C_L}t$$

The rate at which the output voltage decreases

$$\frac{dv_O}{dt} = -\frac{i_L}{C_L} = -\frac{10^{-9}}{10^{-12}} = -1000\text{ V/s} \Rightarrow -1\text{ V/ms}$$

the capacitor would completely discharge in 4 ms.

Example 16.14 **Objective:** Determine the output of an NMOS inverter driven by a series of NMOS transmission gates.

Consider the circuit shown in Figure 16.58. The NMOS inverter is driven by three NMOS transmission gates in series. Assume the threshold voltages of the n-channel transmission gate transistors and the driver transistor are $V_{TN} = +0.8\,V$, and the threshold voltage of the load transistor is $V_{TNL} = -1.5\,V$. Let $K_D/K_L = 3$ for the inverter. Determine v_O for $v_I = 0$ and $v_I = 5\,V$.

Solution: The three NMOS transmission gates in series act as an AND/NAND function. If $v_I = 0$ and $A = B = C =$ logic $1 = 5\,V$, the gate capacitance to driver M_D becomes completely discharged, which means that $v_{O1} = v_{O2} = v_{O3} = 0$. Driver M_D is cut off and $v_O = 5\,V$.

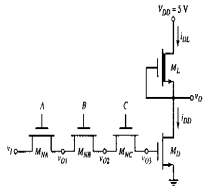


Figure 16.58 NMOS inverter driven by three NMOS transmission gates in series

If $v_I = 5\,V$ and $A = B = C =$ logic $1 = 5\,V$, the three transmission gates are biased in their conducting state, and the gate capacitance of M_D becomes charged. For transistor M_{NA}, the current becomes zero when the gate-to-source voltage is equal to the threshold voltage, or, from Equation (16.87(b)),

$$v_{O1} = V_{DD} - V_{TN} = 5 - 0.8 = 4.2\,V$$

Transistors M_{NB} and M_{NC} also cut off when the gate-to-source voltages are equal to the threshold voltage; therefore,

$$v_{O2} = v_{O3} = V_{DD} - V_{TN} = 5 - 0.8 = 4.2\,V$$

This result shows that the drain-to-source voltages of M_{NB} and M_{NC} are also zero. A threshold voltage drop is lost in the first transmission gate, but additional threshold voltage drops are not lost in subsequent NMOS transmission gates in series.

For a voltage of $v_{O3} = 4.2\,V$ applied to the gate of M_D, the driver is biased in the nonsaturation region and the load is biased in the saturation region. From $i_{DD} = i_{DL}$, we have

$$K_D[2(v_{O3} - V_{TN})v_O - v_O^2] = K_L[-V_{TNL}]^2$$

The output voltage is found to be

$$v_O = 0.112\,V$$

If any one of the transmission gate voltages, A or B or C, switches to a logic 0, then v_{O3} will begin to discharge through a reverse-biased pn junction in the transmission gates, which means that v_O will increase with time.

Comment: In this example, the inverter is again in a dynamic condition; that is, when any transmission gate is cut off, the output voltage changes with time. However, this type of circuit can be used in clocked digital systems.

Test Your Understanding

16.26 The threshold voltage of the NMOS transmission gate transistor in Figure 16.55(a) is $V_{TN} = 1\,V$. Determine the quiescent output voltage v_O for: (a) $v_I = \phi = 5\,V$; (b) $v_I = 3\,V$, $\phi = 5\,V$; (c) $v_I = 4.2\,V$, $\phi = 5\,V$; and (d) $v_I = 5\,V$, $\phi = 3\,V$. (Ans. (a) $v_O = 4\,V$ (b) $v_O = 3\,V$ (c) $v_O = 4\,V$ (d) $v_O = 2\,V$)

16.26 on page 1062.

Given that

$V_{TN} = 1V$

Determine V_O for

(a) $V_I = \phi = 5V$

(b) $V_I = 3V$, $\phi = 5V$

(c) $V_I = 4.2V$, $\phi = 5V$

Sol:

(a) When $V_I = \phi$

$V_I = 5V$

$\phi = 5V$

⇒ The transmission gate is biased in conducting state and the gate capacitance becomes fully charged when $V_{GS} = V_{TN}$

⇒ Equation 16.87b can be used

⇒ $V_O = V_{DD} - V_{TN}$ $\quad V_{DD} = \phi$

⇒ $V_O = 5 - 1 = 4V$

$V_O = 4V$

(b) When $V_I = 3V$

$\phi = 5V$

⇒ As we know in NMOS transmission gate when $V_I \le V_{DD} - V_{TN}$, the output follow input i.e $V_O = V_I$ Since $V_I < 4.2$

In given case

$V_O = 3V$

(c) When

$V_I = 4.2V$

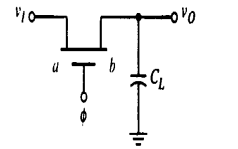
$\phi = 5V$

In this case

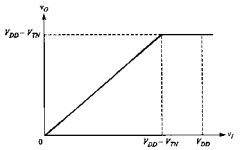
$V_I = V_{DD} - V_{TN}$

⇒ $V_I = 5 - 1 = 4V$

$V_I = 4V$

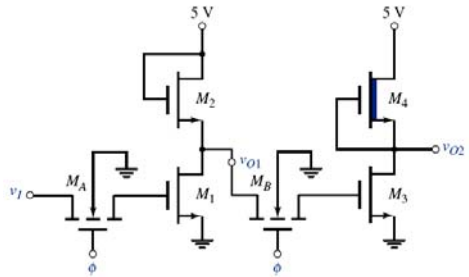


$V_O(max) = V_{DD} - V_{TN}$



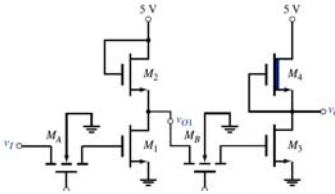
Example 16.52 p1106

D16.52 For the circuit in Figure P16.52, the input voltage v_I is either 0.1 V or 5 V. Let $\phi = 5\,V$. The threshold voltages are $V_{TN} = -1.5\,V$ for M_4 and $V_{TN} = 0.8\,V$ for all other transistors. The width-to-length ratios are 1 for M_2 and M_4 and 10 for M_A and M_B. (a) What are the logic 1 values of v_{O1} and v_{O2}? (b) Design the width-to-length ratios of M_1 and M_3 such that the logic 0 values of v_{O1} and v_{O2} are 0.1 V. **Neglect the body effect.**



(a) v_{O1}(logic 1) = 4.2 V, v_{O2}(logic 1) = 5 V

Example 16.52 p1106



(b) $v_I = 5\text{ V} \Rightarrow v_{GS1} = 4.2\text{ V}$

M_1 in nonsaturation and M_2 in saturation.

NMOS Inverter with Enhancement Load

$$K_D[2(v_I - V_{TND})v_O - v_O^2] = K_L(V_{DD} - v_O - V_{TNL})^2$$

$$\left(\frac{W}{L}\right)_D[2(v_{GS1} - V_{TND})v_{O1} - v_{O1}^2] = \left(\frac{W}{L}\right)_L(V_{DD} - v_{O1} - V_{TNL})^2$$

$$\left(\frac{W}{L}\right)_D[2(4.2 - 0.8)(0.1) - (0.1)^2] = (1)[5 - 0.1 - 0.8]^2 \quad \left(\frac{W}{L}\right)_D(0.67) = 16.81 \Rightarrow \left(\frac{W}{L}\right)_D = 25.1$$

Now $v_{O1} = 4.2\text{ V} \Rightarrow v_{GS3} = 4.2\text{ V}$

M_3 in nonsaturation and M_4 in saturation.

NMOS Inverter with Depletion Load

$$\frac{K_D}{K_L}[2(v_I - V_{TND})v_O - v_O^2] = (-V_{TNL})^2$$

$$\left(\frac{W}{L}\right)_D[2(v_{GS3} - V_{TND})v_{O2} - v_{O2}^2] = \left(\frac{W}{L}\right)_L[-V_{TNL}]^2$$

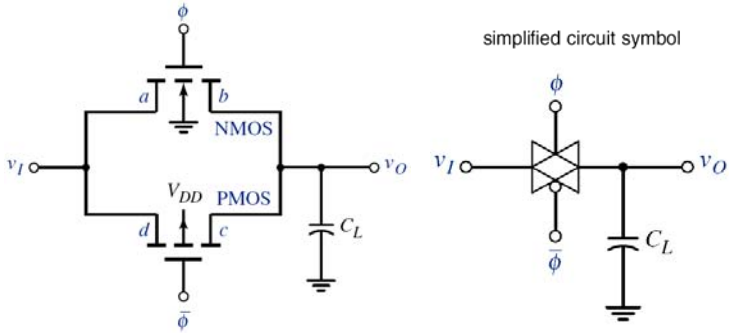
$$\left(\frac{W}{L}\right)_D[2(4.2 - 0.8)(0.1) - (0.1)^2] = (2)[-(-1.5)]^2$$

$$\left(\frac{W}{L}\right)_D(0.67) = 2.25$$

$$\left(\frac{W}{L}\right)_D = 3.36$$

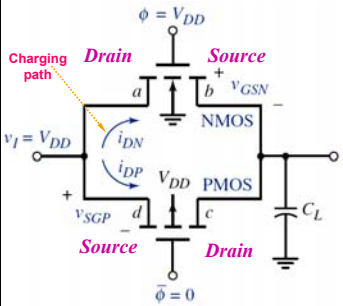
CMOS Transmission Gate

- A CMOS transmission gate can be constructed by parallel combination of NMOS and PMOS transistors, with complementary gate signals.
- The main advantage of the CMOS transmission gate compared to NMOS transmission gate is to allow the input signal to be transmitted to the output **without the threshold voltage attenuation**.



CMOS Transmission Gate

Case I: Input High condition



If $\phi = V_{DD}$, $\bar{\phi} = 0$, $v_I = V_{DD}$, and v_O is initially zero,

NMOS terminal *a* acts as the drain
terminal *b* acts as the source

PMOS terminal *c* acts as the drain
terminal *d* acts as the source

In order to charge the load capacitor, current enters the NMOS drain and the PMOS source.

NMOS $v_{GSN} = \phi - v_O = V_{DD} - v_O$

V_{GSN} continuously change

PMOS $v_{SGP} = v_I - \bar{\phi} = V_{DD} - 0 = V_{DD}$

V_{GSP} remains constant

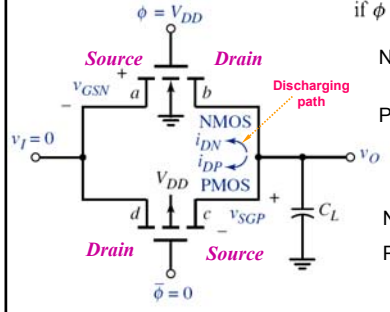
when $v_O = V_{DD} - V_{TN}$, the NMOS cuts off and $i_{DN} = 0$ since $v_{GSN} = V_{TN}$. PMOS continues to conduct since $v_{SGP} = V_{DD}$

In PMOS, I_{DP}=0, when V_{SDP}=0, which would be possible only, if, V_O=V_I=5V

logic '1' is unattenuated

CMOS Transmission Gate

Case II: Input Low condition



if $\phi = V_{DD}$, $\bar{\phi} = 0$, $v_I = 0$, and $v_O = V_{DD}$ initially

NMOS terminal *a* acts as the source
terminal *b* acts as the drain

PMOS terminal *c* acts as the source
terminal *d* acts as the drain

In order to discharge the load capacitor, current enters the NMOS drain and the PMOS source.

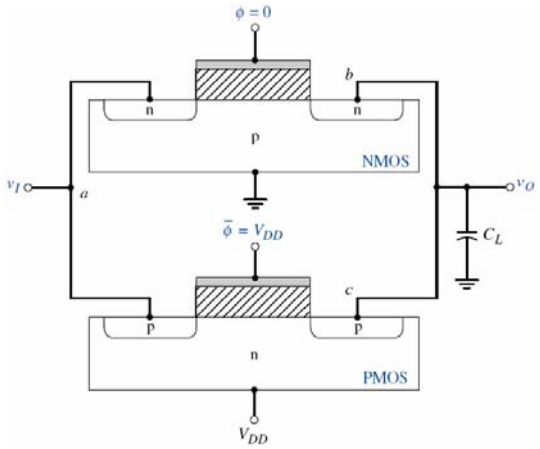
NMOS $v_{GSN} = \phi - v_I = V_{DD} - 0 = V_{DD}$

PMOS $v_{SGP} = v_O - \bar{\phi} = v_O - 0 = v_O$

When $v_{SGP} = v_O = |V_{TP}|$, the PMOS device cuts off and i_{DP} goes to zero. However, since $v_{GSN} = V_{DD}$, the NMOS transistor continues conducting and capacitor C_L completely discharges to zero.

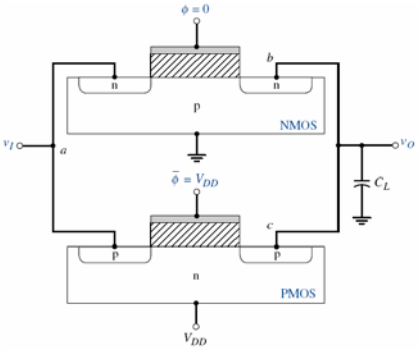
Finally, V_O=0, which is **a good logic 0**. $v_{SGP} = v_o - \bar{\phi} = v_o - 0 = v_o$

CMOS Transmission Gate



CMOS Transmission Gate

CMOS transmission gate remains in a dynamic condition.



- If *VO=VDD and ϕ=0*, then NMOS substrate to terminal 'b' pn junction is reverse biased and capacitor CL can discharge.
- If *VO=0,* then the PMOS terminal c-to-substrate pn junction is reverse biased and capacitance CL can be charge to a positive voltage.
- ***This implies that the output high or low of CMOS transmission gate circuit do not remain constant with time (dynamic behavior).***

Test your understanding p1067

16.29 Consider the CMOS transmission gate in Figure 16.64(a). Assume transistor parameters of $V_{TN} = +0.8\,\text{V}$ and $V_{TP} = -1.2\,\text{V}$. When $\phi = 5\,\text{V}$, input v_I varies with time as $v_I = 0.5t\,\text{V}$ for $0 \le t \le 10\,\text{s}$. Let $v_O(t = 0) = 0$ and assume $C_L = 1\,\text{pF}$. Determine the range of times that the NMOS and PMOS devices are conducting or cut off.

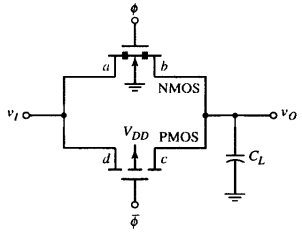
Exercise 16.29 (a) p10XX

Given that V_{TN}=**0.8V**, V_{TP}=**-1.2V**. When ϕ = **5V**, input v_I varies with time as v_I =**0.5***t* for **0** $\le t \le$ **10 sec**. Let V_O=**0** and C_L=**1pF**. Determine the range of the times that the NMOS and PMOS devices are conducting or cutoff.

NMOS conducting for $0 \le v_I \le 4.2\text{V}$

NMOS conducting for $0 \le t \le 8.4$ **sec**

NMOS cutoff for $8.4 \le t \le 10$ **sec**



HW solution

EX16.8

(a) $V_{II} = \dfrac{V_{DD}}{2} = \dfrac{2.1}{2} = 1.05 \text{ V}$

$V_{OPt} = V_{II} - V_{TD} = 1.05 - (-0.4) = 1.45 \text{ V}$

$V_{ONt} = V_{II} - V_{TN} = 1.05 - 0.4 = 0.65 \text{ V}$

(b) $V_{II} = \dfrac{2.1 + (-0.4) + \sqrt{0.5}(0.4)}{1 + \sqrt{0.5}} = 1.16 \text{ V}$

$V_{OPt} = 1.16 + 0.4 = 1.56 \text{ V}$

$V_{ONt} = 1.16 - 0.4 = 0.76 \text{ V}$

(c) $V_{II} = \dfrac{2.1 + (-0.4) + \sqrt{2}(0.4)}{1 + \sqrt{2}} = 0.938 \text{ V}$

$V_{OPt} = 0.938 + 0.4 = 1.338 \text{ V}$

$V_{ONt} = 0.538 \text{ V}$

TYU16.3

$$P = i_D \cdot V_{DD} \Rightarrow i_D = \frac{800}{5} = 160 \ \mu\text{A}$$

$$i_D = 160 = \frac{35}{2} \cdot \left(\frac{W}{L}\right)_L (1.4)^2 \Rightarrow \underline{\left(\frac{W}{L}\right)_L = 4.66}$$

$$i_D = 160 \ \mu\text{A} = \frac{35}{2} \cdot \frac{1}{3} \cdot \left(\frac{W}{L}\right)_D \left[2(5 - 0.8)(0.12) - (0.12)^2\right] \Rightarrow \underline{\left(\frac{W}{L}\right)_D = 27.6}$$

TYU16.4

a. From the load transistor:

$$I_{DL} = \left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)_L (V_{GSL} - V_{TNL})^2 = \frac{35}{2}(0.5)(5 - 0.15 - 0.7)^2$$

or

$I_{DL} = 150.7 \ \mu\text{A}$

Maximum v_0 occurs when either A or B is high and C is high. For the two NMOS is series, the effective k_N is cut in half, so

$$I_{DL} = \frac{1}{2}\left[\left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)_D\right]\left[2(V_{GSD} - V_{TND})V_{DS} - V_{DS}^2\right]$$

or

$$150.7 = \frac{1}{2}\left[\frac{35}{2} \cdot \left(\frac{W}{L}\right)_D\right]\left[2(5 - 0.7)(0.15) - (0.15)^2\right]$$

which yields

$$\underline{\left(\frac{W}{L}\right)_D = 13.6}$$

b. $P = i_D \cdot V_{DD} = (150.7)(5) \Rightarrow \underline{P = 753 \ \mu\text{W}}$

16.36

a. $V_{0Nt} \le v_{01} \le V_{0Pt}$

By symmetry, $V_{II} = 2.5 \text{ V}$

$V_{0Pt} = 2.5 + 0.8 = 3.3 \text{ V}$

and $V_{0Nt} = 2.5 - 0.8 = 1.7 \text{ V}$

So $\underline{1.7 \le v_{01} \le 3.3 \text{ V}}$

b. For $v_{O2} = 0.6 < V_{TN} \Rightarrow \underline{v_{O3} = 5 \ V}$

N_2 in nonsaturation and P_2 in saturation. From Equation (16.57),

$$\left[2(v_{I2} - 0.8)(0.6) - (0.6)^2\right] = \left[5 - v_{I2} - 0.8\right]^2$$

$$1.2v_{I2} - 1.32 = 17.64 - 8.4v_{I2} + v_{I2}^2$$

or

$$v_{I2}^2 - 9.6v_{I2} + 18.96 = 0$$

So $\underline{v_{I2} = v_{01} = 2.78 \text{ V}}$

For $v_{01} = 2.78$, both N_1 and P_1 in saturation. Then

$\underline{v_I = 2.5 \text{ V}}$

16.39

(a) Switching Voltage, Eq. (16.43)

$$v_{It} = \frac{3.3 - 0.4 + \sqrt{\frac{2(4)}{8}}(0.4)}{1 + \sqrt{\frac{2(4)}{8}}} = 1.65 \text{ V} = v_{It}$$

$$i_{D,\text{peak}} = \left(\frac{80}{2}\right)(4)(1.65 - 0.4)^2 \Rightarrow \underline{i_{D,\text{peak}} = 250 \ \mu\text{A}}$$

(b)

$$v_{It} = \frac{3.3 - 0.4 + \sqrt{\frac{2(4)}{4}}(0.4)}{1 + \sqrt{\frac{2(4)}{4}}} = \underline{1.436 \text{ V} = v_{It}}$$

$$i_{D,\text{peak}} = \left(\frac{80}{2}\right)(4)(1.436 - 0.4)^2 \Rightarrow \underline{i_{D,\text{peak}} = 172 \ \mu\text{A}}$$

(c)

$$v_{It} = \frac{3.3 - 0.4 + \sqrt{\frac{2(4)}{12}}(0.4)}{1 + \sqrt{\frac{2(4)}{12}}} \Rightarrow \underline{v_{It} = 1.776 \text{ V}}$$

$$i_{D,\text{peak}} = \left(\frac{80}{2}\right)(4)(1.776 - 0.4)^2 \Rightarrow \underline{i_{D,\text{peak}} = 303 \ \mu\text{A}}$$

Chapter 16

MOSFET Digital Circuits

Chapter 16.7

Sequential Logic Circuit

SEQUENTIAL LOGIC CIRCUITS

In the logic circuits that we have considered in the previous sections, such as NOR and NAND logic gates, the output is determined only by the instantaneous values of the input signals. These circuits are therefore classified as combinational logic circuits.

Another class of circuits is called **sequential logic circuits**. The output depends not only on the inputs, but also on the previous history of its inputs.

This feature gives sequential circuits the property of memory. Shift registers and flip-flops are typical examples of such circuits. We will also briefly consider a full-adder circuit. The characteristic of these circuits is that they store information for a short time until the information is transferred to another part of the system.

SEQUENTIAL LOGIC CIRCUITS

- The logic circuits considered thus far are called **combinational logic circuits**. Their output depend only on the present value of input. This implies that these circuit do not have ***memory.***
- Another class of the logic circuit that incorporate memory are called ***sequential logic circuits***; that is, their output depend not only the present value of the input, but also on the previous history of inputs. ***Shift registers*** and ***flip-flops*** are typical examples of such circuits.

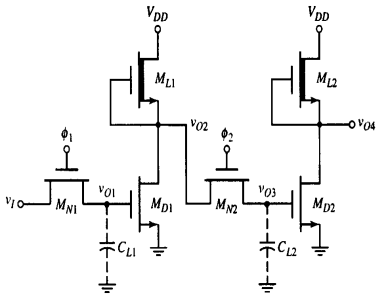
SEQUENTIAL LOGIC CIRCUITS

NMOS Dynamic Shift Registers

- A shift register can be constructed by the combination of transmission gates and inverters.
- If $V_I=V_{DD}$ and $\phi_1=V_{DD}$, then a logic 1=V_{DD}-V_{TN} would exist at V_{O1}.
- The C_L charges through M_{N1}.

As V_{O1} goes high, V_{O2} goes low.

If ϕ_2 is high low will transmitted through M_{N2} and V_{O4} would be at logic 1. Thus logic 1 ***shifted*** from input to output.



In shift register the input signal is transmitted, or shifted, from the input to the output during one clock cycle.

Dynamic Shift Registers at Various Time

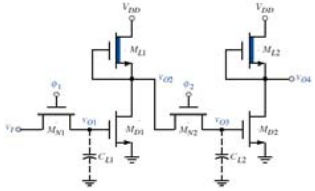
Suppose V_{DD}=5V and V_{TN}=1V.

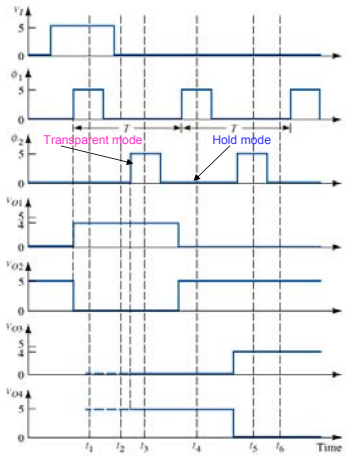
At t=t_1 , V_1=ϕ_1=5V, v_{O2} goes low

At this time M_{N2} is still in cutoff (ϕ_2=0)

even though input of M_{N2} has been changed. This implies that v_{O3} and v_{O4} depend on the ***previous history***.

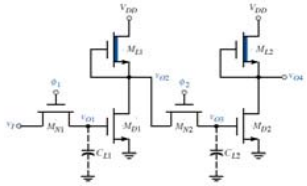
Similarly at t=t_3, ϕ_2 is high, and logic 0 at v_{O2} is transmitted to v_{O3}, which force v_{O4} to 5V. Thus the input information is transmitted to output during one clock cycle.

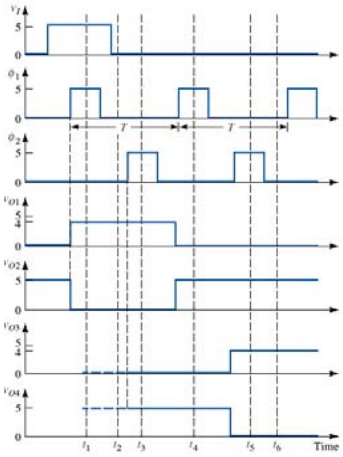




Dynamic Shift Registers at Various Time

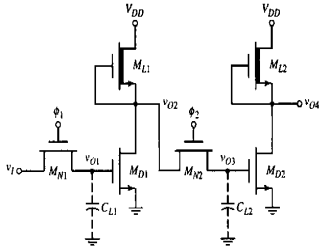
- Consider when t=t_4, v_I=0, and ϕ1=5V, so V_{O1}=0 and V_{O2}=5V.Vo_3 and Vo_4 depend on previous history
- At t=t_5, ϕ_2=5V, v_{O3} charges to V_{DD}-V_{TN}=4V and V_{O4} goes low.
- Thus logic 0 is shifted (transmitted) from input to output.
- Also note that v_{O3} and v_{O4} are depend on previous history of their inputs instead of current inputs (they are having memory).





NMOS shift register is also dynamic (why?)

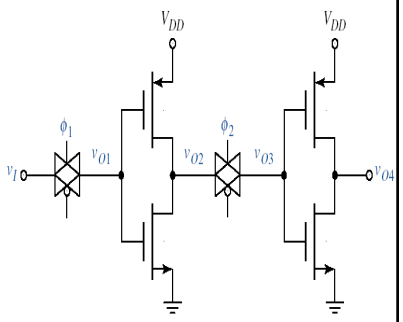
- The output charged capacitor does not remain constant with time because it is discharge through the transmission gate transistor.
- In order to prevent logic errors, the clock signal period T must be small compared to effective RC discharge time constant.



For example at t = t_2, V_{O1}=4V, ϕ_1=0 and M_{N1} is cutoff.V_{O1} will start to to decay and V_{O2} will begin to increase.

CMOS Dynamic Shift Registers

- The operation of the CMOS shift register is similar to the NMOS register except for the voltage levels.
- For example, when $v_I=\phi_1=V_{DD}$. Then $v_{O1}=V_{DD}$ and $v_{O2}=0$. when ϕ_2 goes high, then v_{o3} switch to zero, $v_{o4}=v_{DD}$.
- Thus input signal is shifted to the output during one clock cycle.

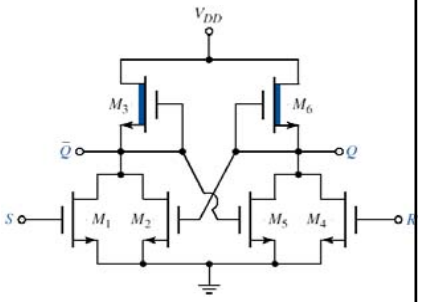


NMOS R-S Flip Flop

- Flip- flops are **bistable** circuits usually formed by cross-coupling two NOR gates. The output of the two NOR circuits are connected back to the inputs of the opposite NOR gates.

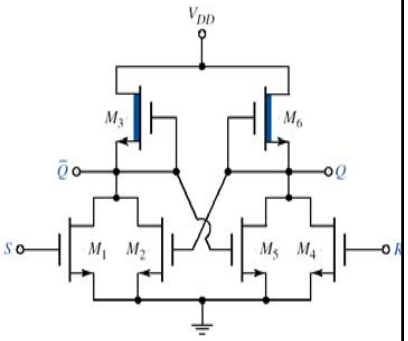
When S=logic 1 and R=logic 0 $\bar{Q}$ =logic 0 and Q=logic 1=V_{DD} Transistor M_2 is then also biased in conducting state.

If S returns to logic 0, nothing in the circuit can force a change and flip flop stores the previous logic states, although M_1 turned off (but M_2 remains tuned on).



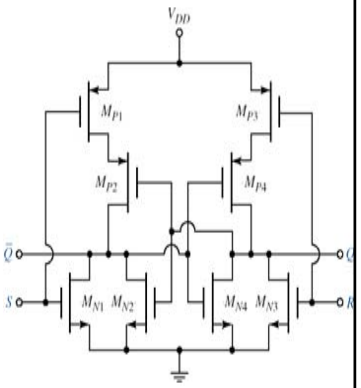
NMOS R-S Flip Flop (cont.)

- When R=logic 1 and S=logic 0
- Then M_4 turn on so output goes low. With S=Q=Logic 0, both M_1 and M_2 are cutoff and goes high. The flip-flop is now in reset state.
- If both S and R inputs go high. Then both outputs Q and $\bar{Q}$ would go low, which implies that output is not complementary This condition is forbidden or nonallowed condition.



CMOS R-S Flip-Flop

- The operation sequence of CMOS R-S flip flop is same as NMOS.
- For example: If S = logic 1 and R = logic 0, then M_{N1}, is turned on, M_{p1}, is cut off, and $\bar{Q}$ goes low.
- With $\bar{Q}$ = R = logic 0, then both M_{N3} and M_{N4} are cut off, both M_{p3} and M_{p4} are biased in a conducting state so that the output Q goes high.
- With Q = logic 1, M_{N2} is biased on, M_{p2} is biased off, and the flip-flop is in a set condition.
- When S goes low, M_{N1}, turns off, but M_{N2} remains conducting, so the state of the flip-flop does not change.



CMOS R-S Flip-Flop (cont.)

- When S = logic 0 and R = logic 1, then output Q is forced low, output $\bar{Q}$ goes high, and the flip-flop is in a reset condition.
- Again, a logic 1 at both S and R is considered to be a forbidden or a nonallowed condition, since the resulting outputs are not complementary.

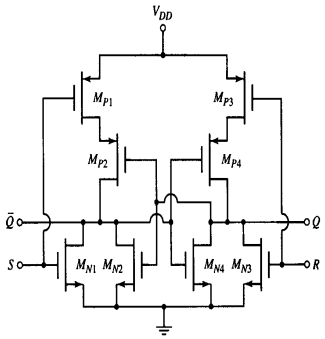


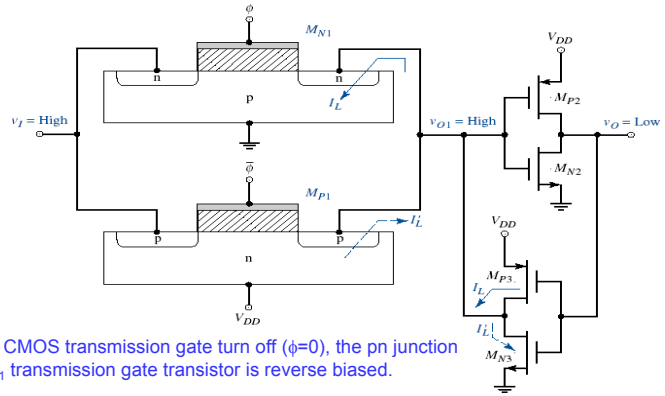
Figure 16.72 CMOS R–S flip-flop

Static vs Dynamic Storage

- Static storage
  - preserve state as long as the power is on
  - have positive feedback (regeneration) with an internal connection between the output and the input
  - useful when updates are infrequent (clock gating)
- Dynamic storage
  - store state on parasitic capacitors
  - only hold state for short periods of time (milliseconds)
  - require periodic refresh
  - usually simpler, so higher speed and lower power

Static D-type Flip-Flop

- A D-type flip-flop is used to provide a delay. The logic bit on the D input is transferred to the output at the next clock pulse.



When the CMOS transmission gate turn off (ϕ=0), the pn junction in the M_{N1} transmission gate transistor is reverse biased.

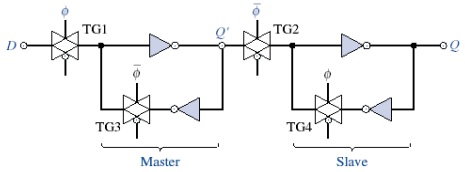


Figure 16.74 CMOS master–slave D flip-flop

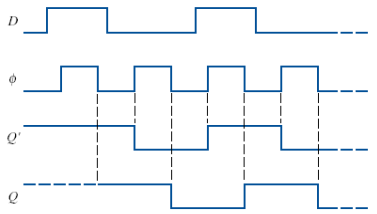


Figure 16.75 D flip-flop signals at various times