ECE 424 – INTRODUCTION TO VLSI DESIGN + LAB

LABORATORY WORK 2

In this laboratory work, we will try to design NMOS circuits by taking the advantage of knowing how to use pspice. That is why first lab homework was very important.

NMOS INVERTERS:

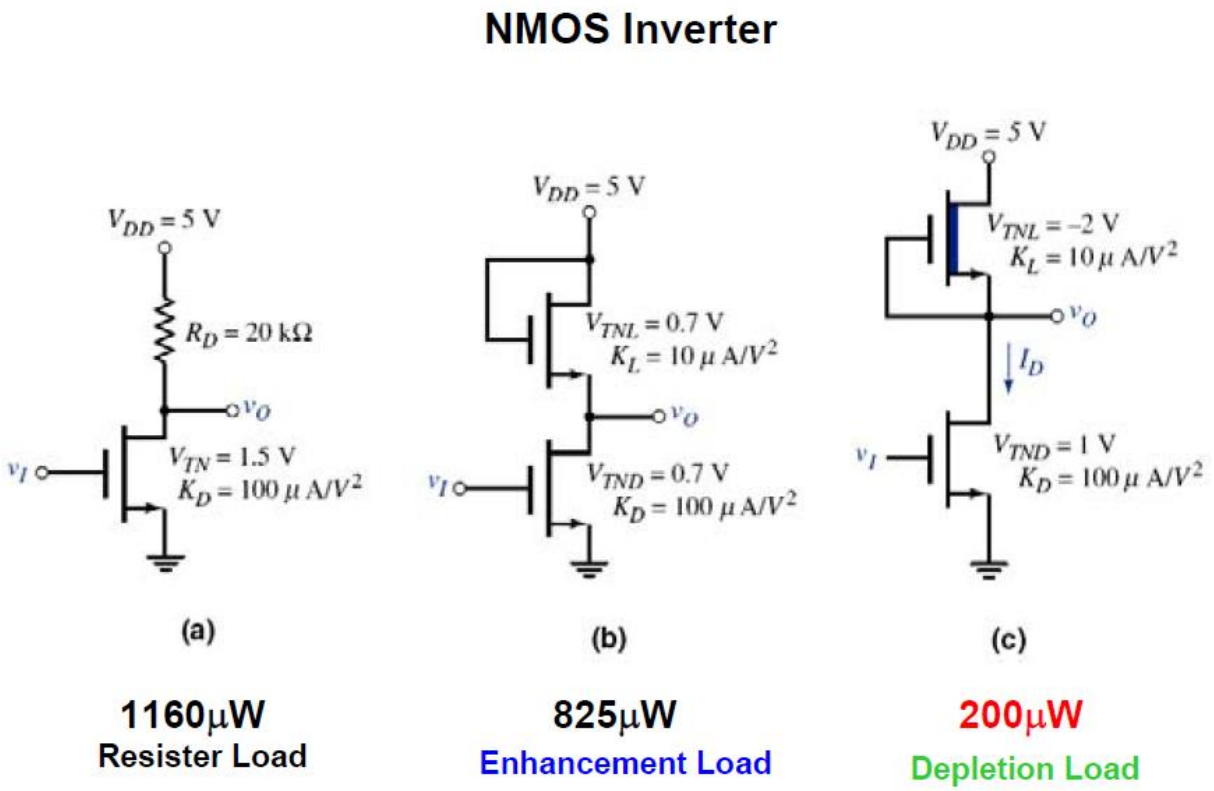


Figure 1

The circuits shown in Figure 1 are taken from the lecture notes. They are different types of inverters. You had studied on first one (Resistor Load).

1. Construct "Enhancement Load" inverter circuit by using ORCAD. Take V_{DD}=5V and don't forget to connecting ground. Fill the following tables by taking notes on a paper.

Vin	Vout
0 V	
5 V	

Vin	0V	0.5V	1V	1.5V	2V	2.5V	3V	3.5V	4V	4.5V	5V
Vout											

After you have finished filling these tables, draw the Voltage Transfer Characteristic of this NMOS inverter by using simulation property of ORCAD.

The previous experiment is teaching you NMOS logic families and their implementation in inverter form. Now we will try to design multi-input NMOS logic circuits.

NMOS NOR GATE:

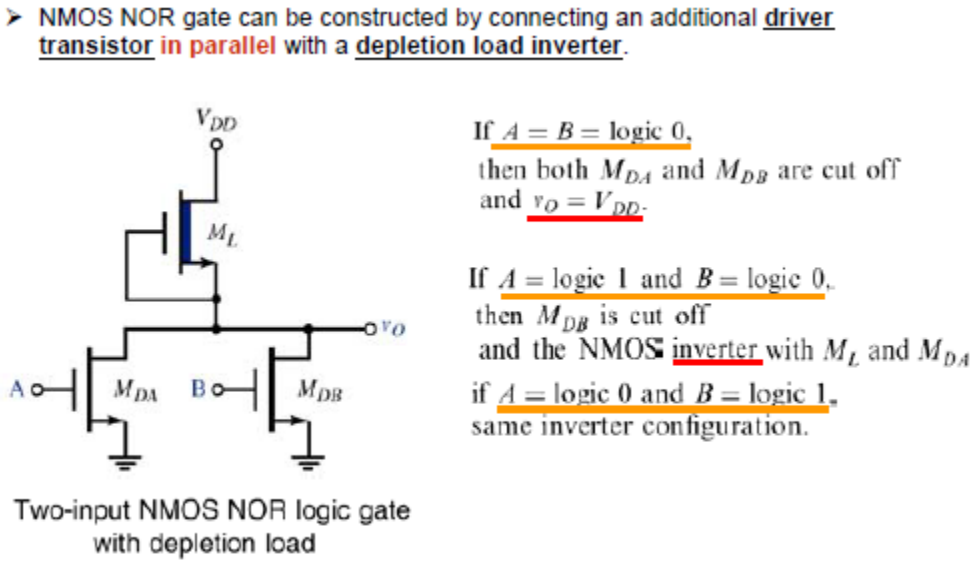
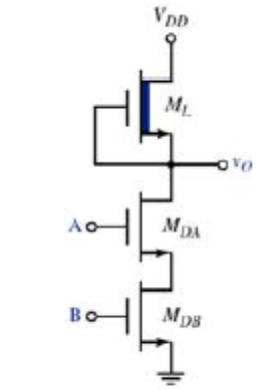


Figure 2

2. The circuit which is given in figure 2 is a NMOS NOR logic gate. The working principle of this circuit is also given at right side of the circuit. Construct that circuit by using ORCAD and try to fill the table below by taking notes on a paper. Compare your results with theoretical ones. (Logic 0=0V, Logic 1=5V)

A	B	Vo
0	0	
0	1	
1	0	
1	1	

NMOS NAND GATE:



Two-input NMOS NAND logic gate with depletion load

If both $A = B =$ logic 0, or if either A or B is a logic 0, at least one driver is cut off, and the output is high.

If both $A = B =$ logic 1, then the composite driver of the NMOS inverter conducts and the output goes low.

Figure 3

3. NMOS NAND Logic gate circuit is given above. Construct that circuit by using ORCAD and try to fill the table below by taking notes on a paper. Compare your results with theoretical ones. (Logic 0=0V, Logic 1=5V)

A	B	Vo
0	0	
0	1	
1	0	
1	1	

Homework:

1. Construct NMOS OR and NMOS AND Logic circuits and form a table for each circuit as shown in above. Fill all these tables on a word document. Put this word document into your project folder and zip this folder. **Not just the project file, all project folder should be sent.** Send it to your **laboratory assistant.**

Deadline: 29.10.2013 Tuesday, 21:00.

No late submission is going to be accepted!

2. Make a research on CMOS Circuits and CMOS Logic Design for next laboratory hours.

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