ECE 424 Introduction to VLSI

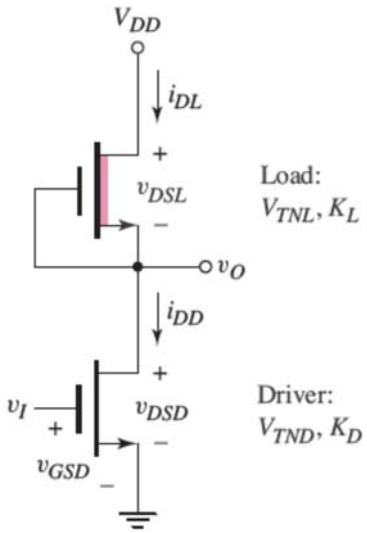
Home Work 1 (Due to 03.11.2014)

NOTE: In the following problems, assume T = 300 K.

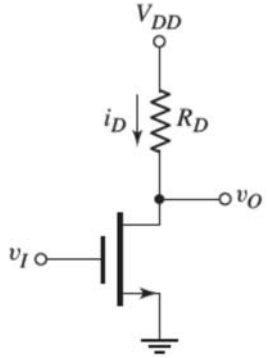
Q1) Plot the I_d versus V_{ds} (for different V_{gs} voltages) characteristics, for an n-channel MOS transistor of L=150nm, W=800 nm, mobility=1830 cm^2/Vs, relative permittivity=11.7, t_{ox}=120 angstrom, using MATLAB. **NOTE:** Print out your results and explanations (including MATLAB codes) for this problem.

Q2) The depletion load NMOS inverter below is biased at V_{DD}=3V. The transistor parameters are $k'_n=60\mu A/V^2$, $(W/L)_D=6$, $(W/L)_L=2$, $V_{TND}=0.4V$, and $V_{TNL}=-0.8V$.

(a) Determine v_o for v_i =3V.
(b) Find the transition points for the driver and the load.
(c) Calculate the power dissipation in the inverter for v_i =3V.



Q3) (a) Redesign the resistive load inverter below so that the maximum power dissipation is 0.25 mW with V_{DD} = 3.3 V and v_O = 0.15 V when the input is a logic 1.
(b) Using the results of part (a), what is the input voltage range when the transistor is biased in the saturation region? Assume transistor parameters of V_{TN} = 0.5 V and k'_n= $100\mu A/V^2$.



Q4) The NMOS inverter with depletion load above is biased at V_{DD} = 2.5 V. The transistor parameters are V_{TND} = 0.5 V and V_{TNL} = −1 V. The width-to-length ratio of the load device is W/L = 1. Assume k'_n= 100μA/V^2.

(a) Design the driver transistor such that v_O = 0.05 V when the input is a logic 1.

(b) What is the power dissipated in the circuit when v_I = 2.5 V?