ECE 424 Introduction to VLSI

Home Work 2 (Due to 17.11.2014)

Q1) For the CMOS inverter below, let VDD = 3.3 V, k′*n*= 100μA/V2, k′*p*= 40μA/V2, V*TN* = 0.4 V, and V*TP* = −0.4 V. Let (W/L)n = 2 and (W/L)p = 5.
(a) (i) Find the transition points for the p-channel and n-channel transistors.
(ii) Sketch the voltage transfer characteristics including the appropriate voltage values at the transition points.
(iii) Find v*I* for v*O* = 0.25 V and v*O* = 3.05 V.
(b) Repeat part (a) for (W/L)n = 4 and (W/L)p = 5.



Q2) The transistor parameters in the CMOS inverter are *VTN* = 0.35 V, *VTP* = −0.35 V, k’n= 80μA/V2, and k’p= 40μA/V2. Let VDD = 1.8 V.
(a) Determine the peak current in the inverter during a switching cycle for (W/L)n = 2 and (W/L)p = 4.
(b) Repeat part (a) for (W/L)n = 2 and (W/L)p = 6.

Q3) Consider the COMS inverter in question 2. A load capacitor of 0.2 pF is connected to the output of a CMOS inverter. Determine the power dissipated in the CMOS inverter for a switching frequency of 10 MHz.

Q4) (a) Determine the noise margins of a CMOS inverter biased at VDD = 3.3V with (W/L)n = 2 and (W/L)p = 5. Assume *VTN* = 0.4 V and *VTP* = −0.4 V.
(b) Repeat part (a) for (W/L)n = 4 and (W/L)p = 12.

Q5) Sketch a stick diagram for the function

Q6) Find the Euler Path and sketch the stick diagram for the function $F=\left(A∙B\right)+\left(C∙D\right)+E$