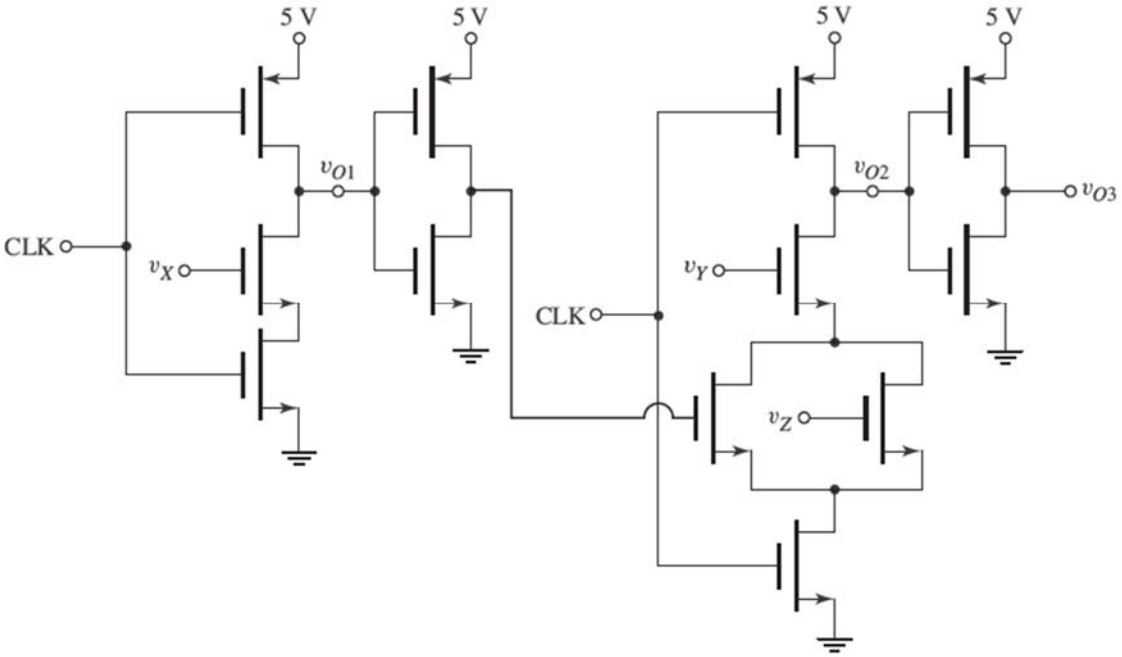
ECE 424 Introduction to VLSI

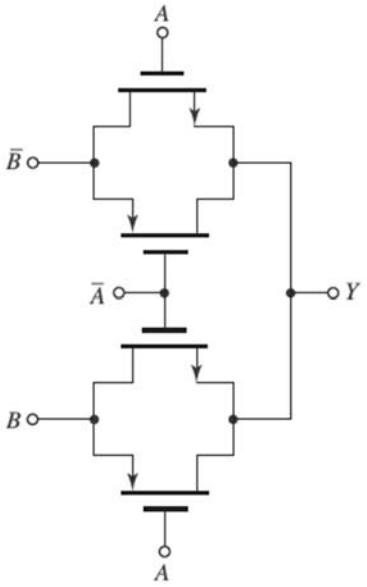
Home Work 3 (Due to the Final Exam)

Q1) (a) For the circuit below, make a table showing the state of each transistor (“on” or “off ”), and determine the output voltages v_{O1}, v_{O2}, and v_{O3} for the input logic states listed in the following table. Assume the input conditions are sequential in time from state 1 to state 6. (b) What logic function does the circuit implement?

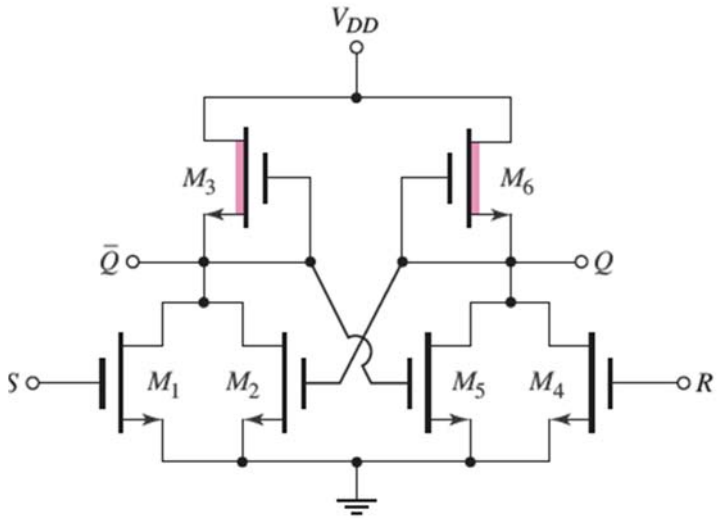
State	CLK	v_X	v_Y	v_Z
1	0	0	0	0
2	1	1	1	1
3	0	0	0	0
4	1	0	1	1
5	0	0	0	0
6	1	1	0	1



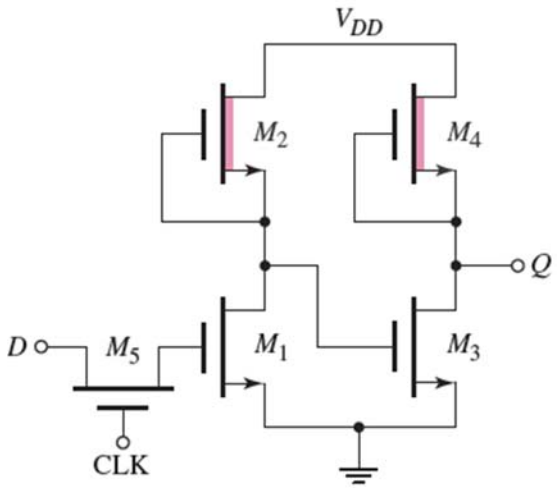
Q2) Consider the circuit below. (a) Determine the value of Y for (i) $A = B = 0$; (ii) $A = 2.5$ V, $B = 0$; (iii) $A = 0$, $B = 2.5$ V; and (iv) $A = B = 2.5$ V. (b) What is the logic function implemented by the circuit?



Q3) Consider the NMOS R-S flip-flop below biased at V_{DD} = 2.5 V. The threshold voltages are 0.4 V (enhancement-mode devices) and −0.6 V (depletion-mode devices). The conduction parameters are $K_3 = K_6 = 40\mu A/V^2$, $K_2 = K_5 = 100\mu A/V^2$, and $K_1 = K_4 = 150\mu A/V^2$. If Q = logic 0 and $\overline{Q}$ = logic 1 initially, determine the voltage at *S* that will cause the flip-flop to change states.



Q4) The circuit below is an example of a D flip-flop. (a) Explain the operation of the circuit. Is this a positive- or negative-edge-triggered flipflop? (b) Redesign the circuit to make this a static flip-flop.



Q5) Show that the circuit below is a J–K flip-flop.