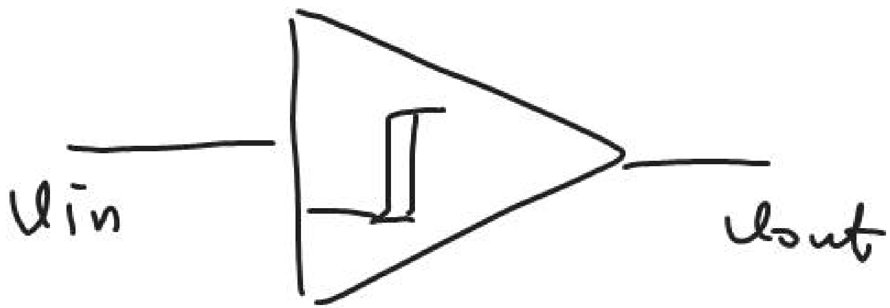
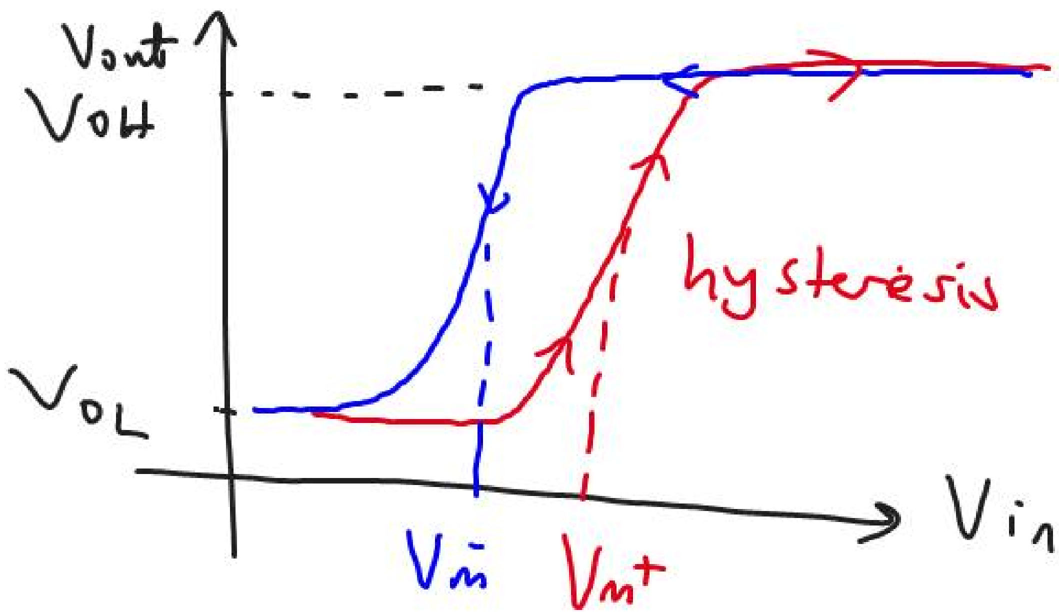
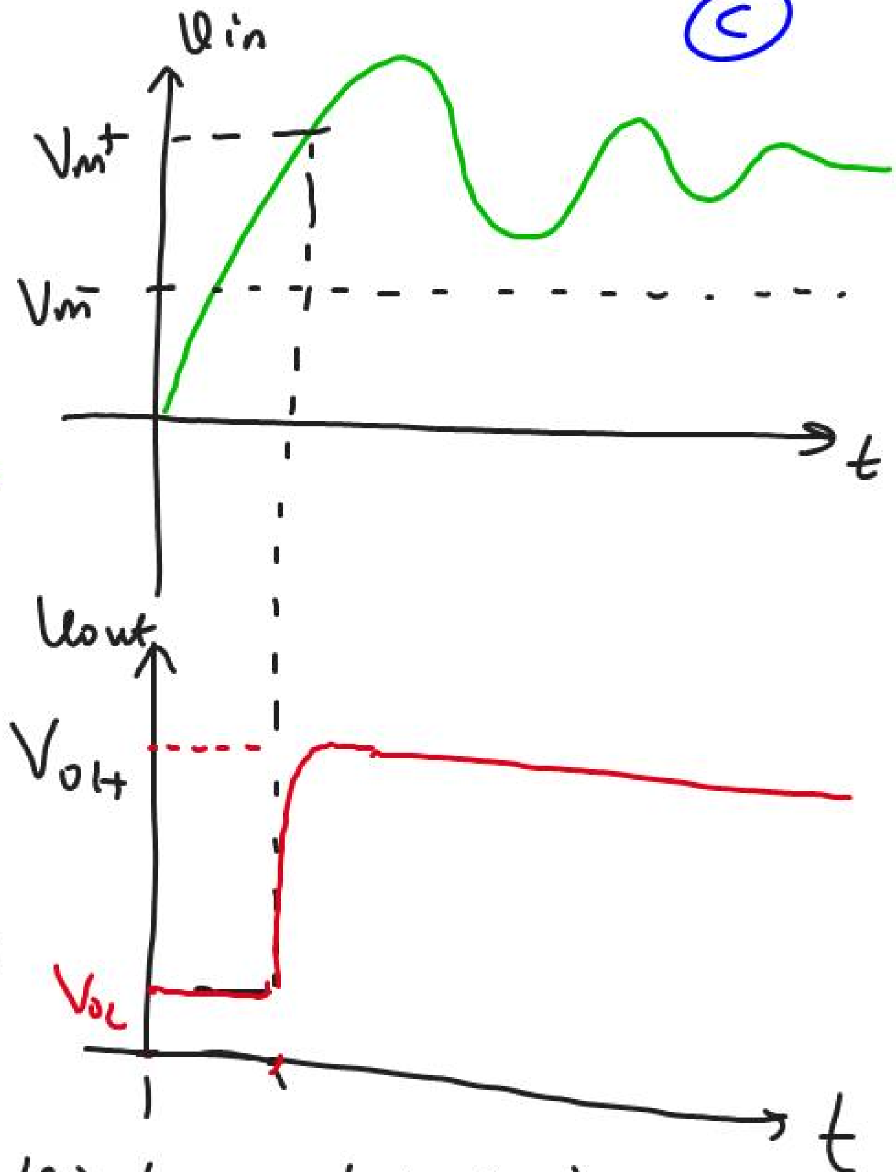
24.12.2010

©

SCHMITT TRIGGER

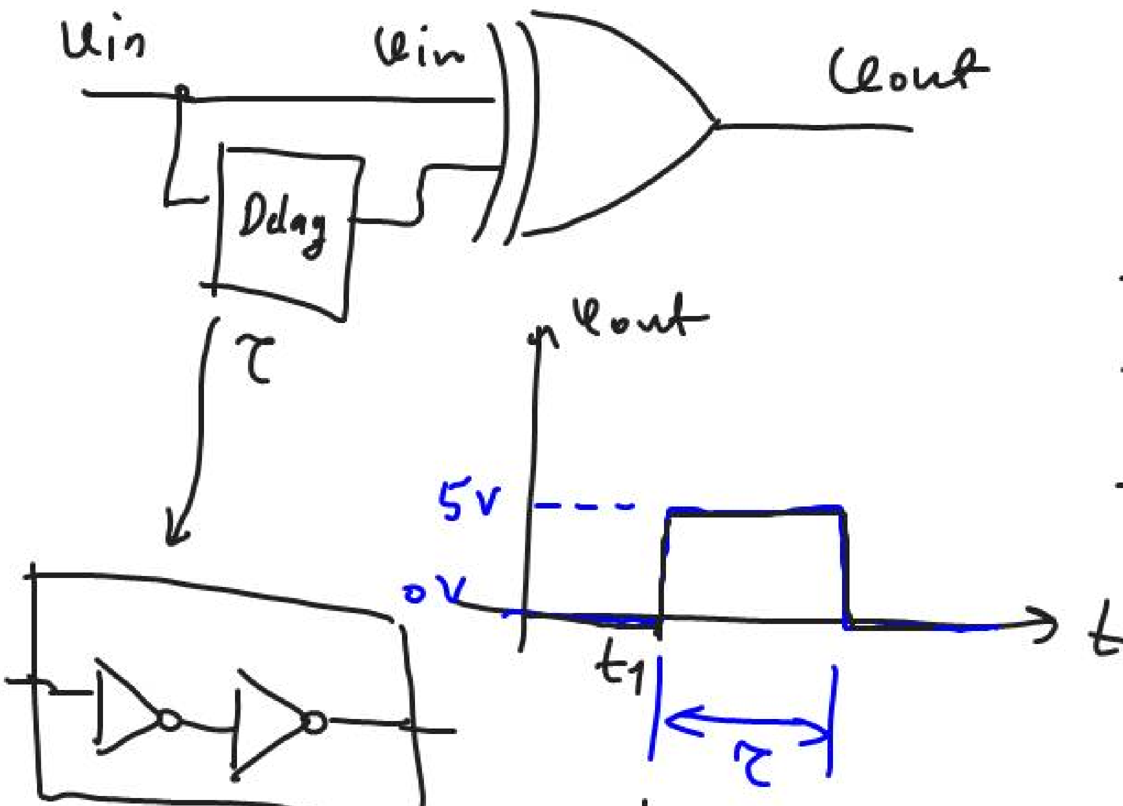






Although V_{in} has a lot of noise, the output signal will be very clean.

MONOSTABLE CIRCUIT

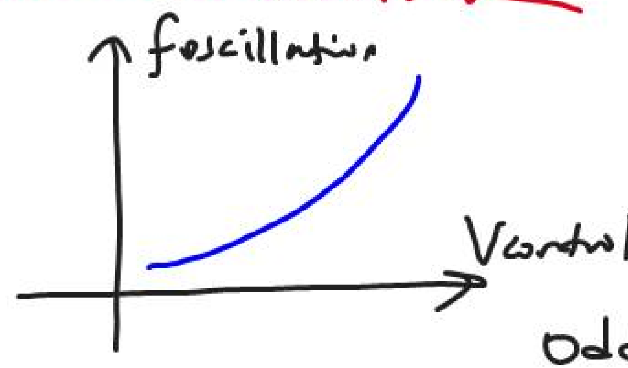


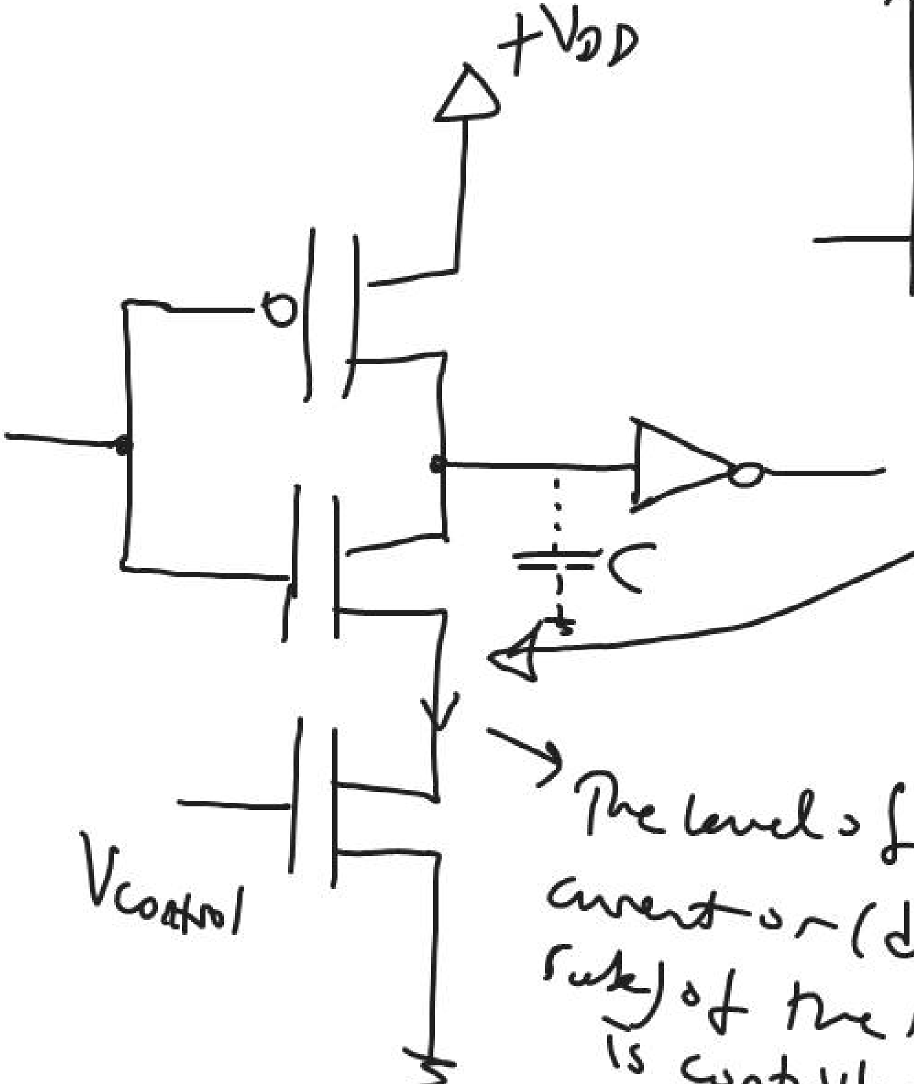
A delay circuit

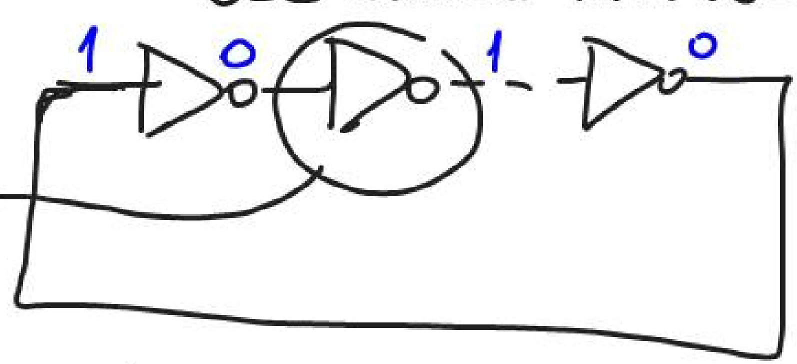
at $t = t_1$ we apply V_{in}

a	b	f
0	0	0
0	1	1
1	0	1
1	1	0

A VOLTAGE-CONTROLLED OSCILLATOR







The level of current or (discharge rate) of the inverter is controlled by $V_{control}$

Astable operation (ring-oscillator)

$T = \frac{1}{f_{osc.}}$

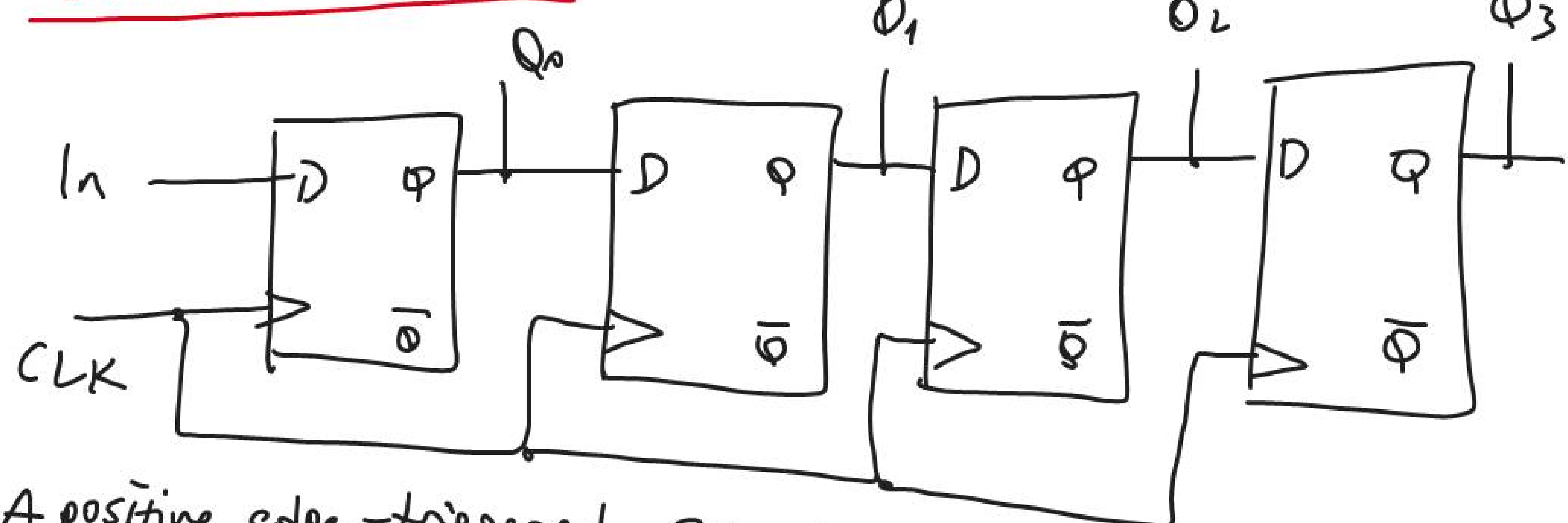
$T = n \cdot t_p$

n: # of inverter

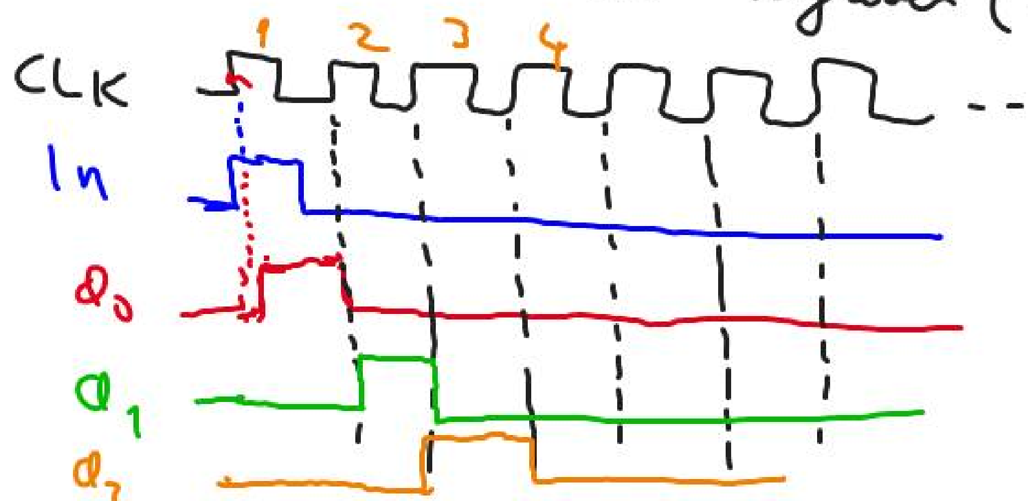
t_p: propagation time of inverter

REGISTERS

SHIFT REGISTER

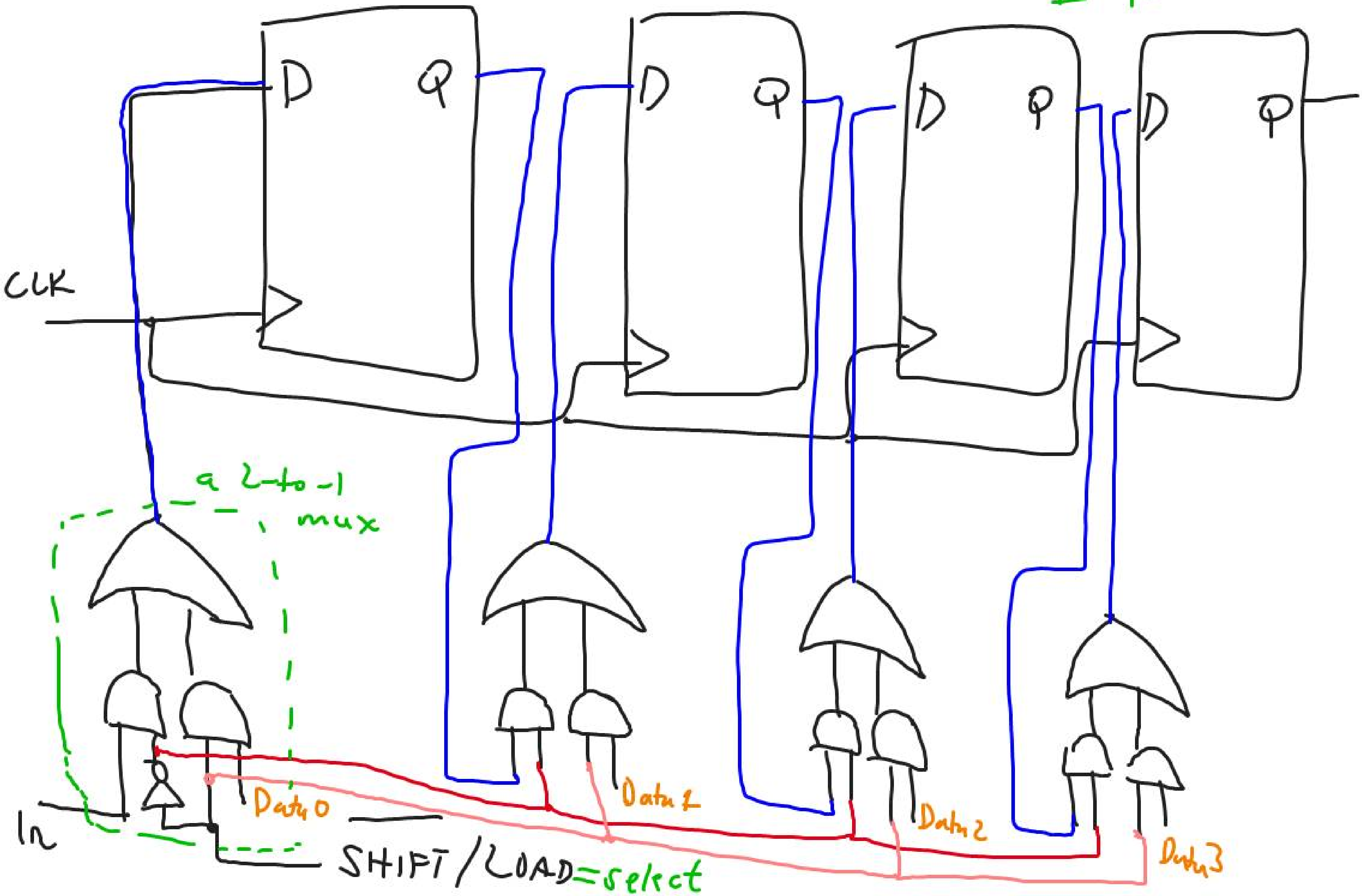


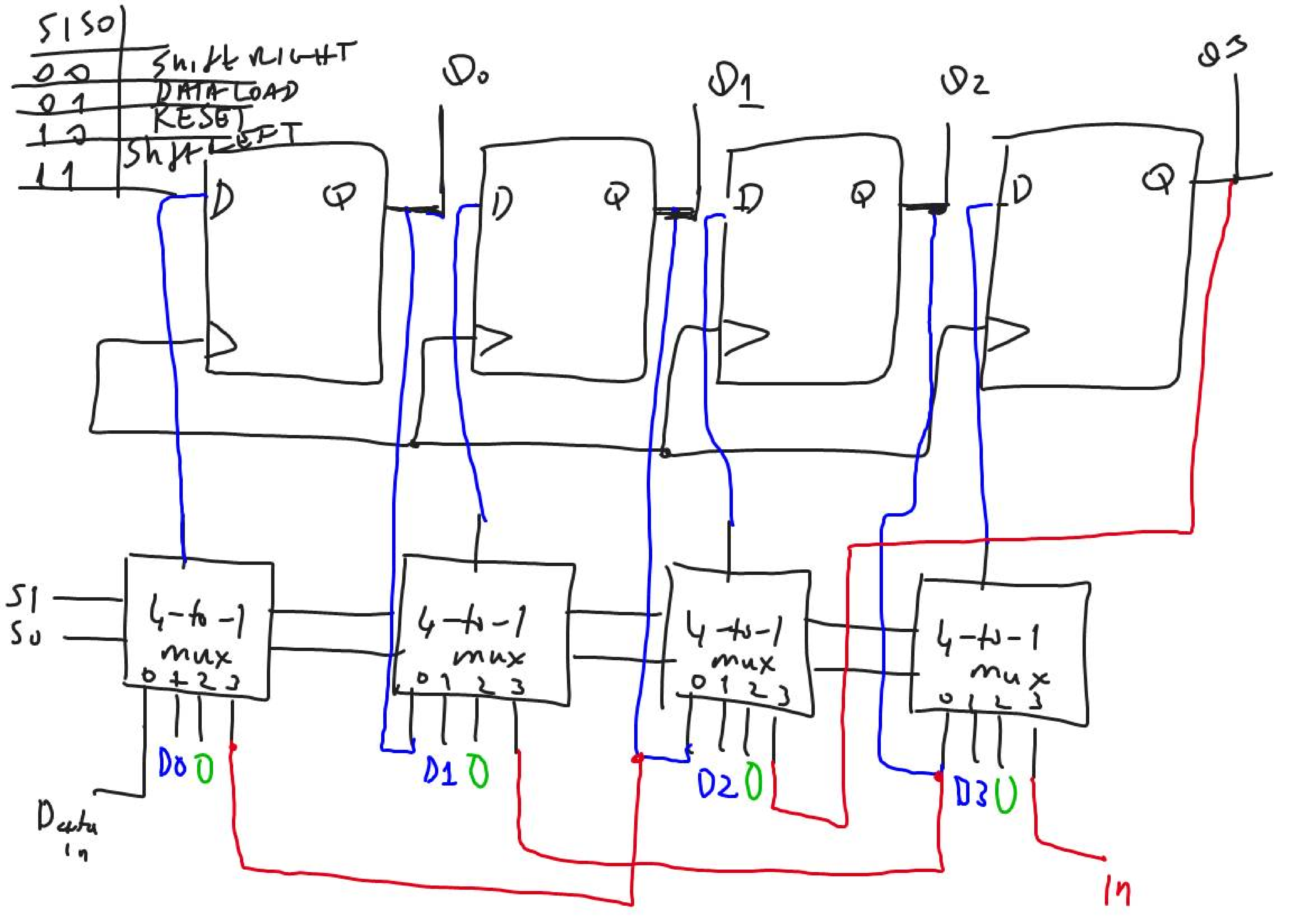
A positive edge-triggered SYNCHRONOUS Register (4-bit)



Shift Right and Data Load register

Select	
0	Shift Right
1	Data LOAD



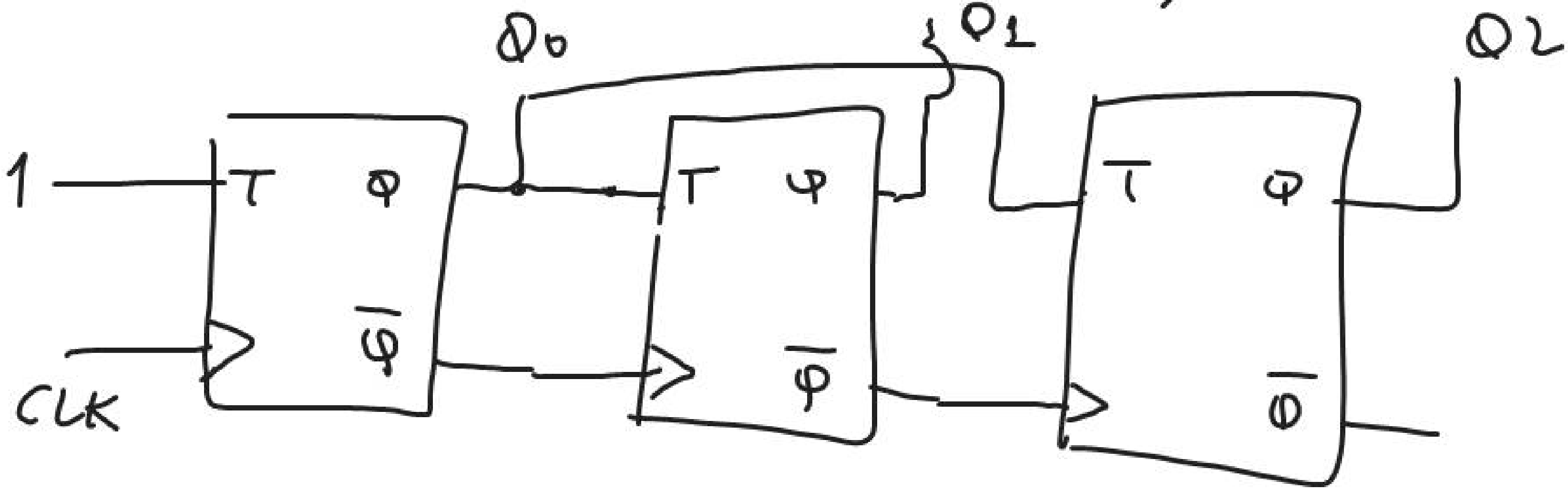


S1 S0
0 0 Shift RIGHT
0 1 DATA LOAD
1 0 RESET
1 1 Shift LEFT
Q0
Q1
Q2
Q3
D
Q
4-to-1 mux
0 1 2 3
S1
S0
D0 0
D1 0
D2 0
D3 0
Data in
In

COUNTERS

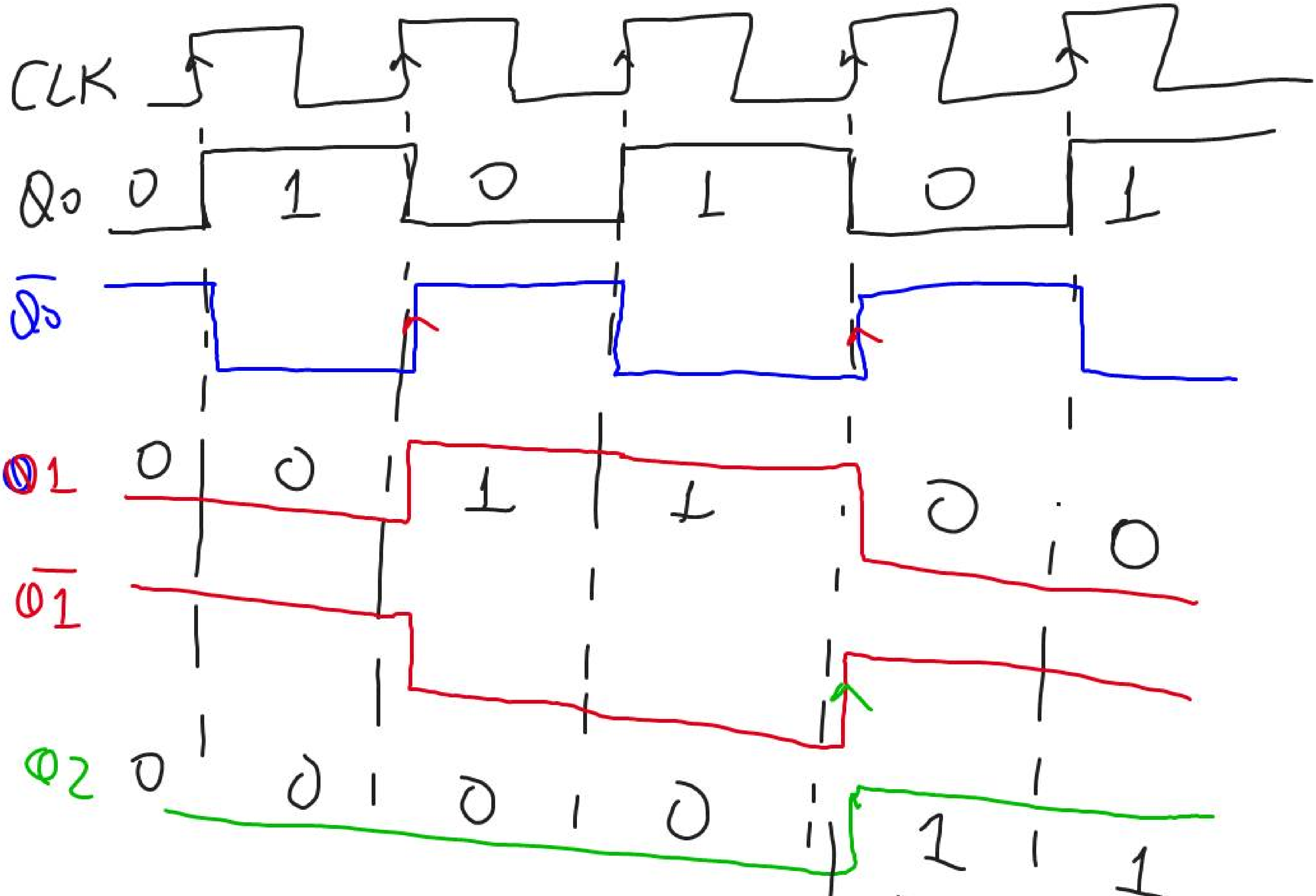
ASSYNCHRONOUS COUNTERS (Ripple Counters)

T flip flops are used. (generally)



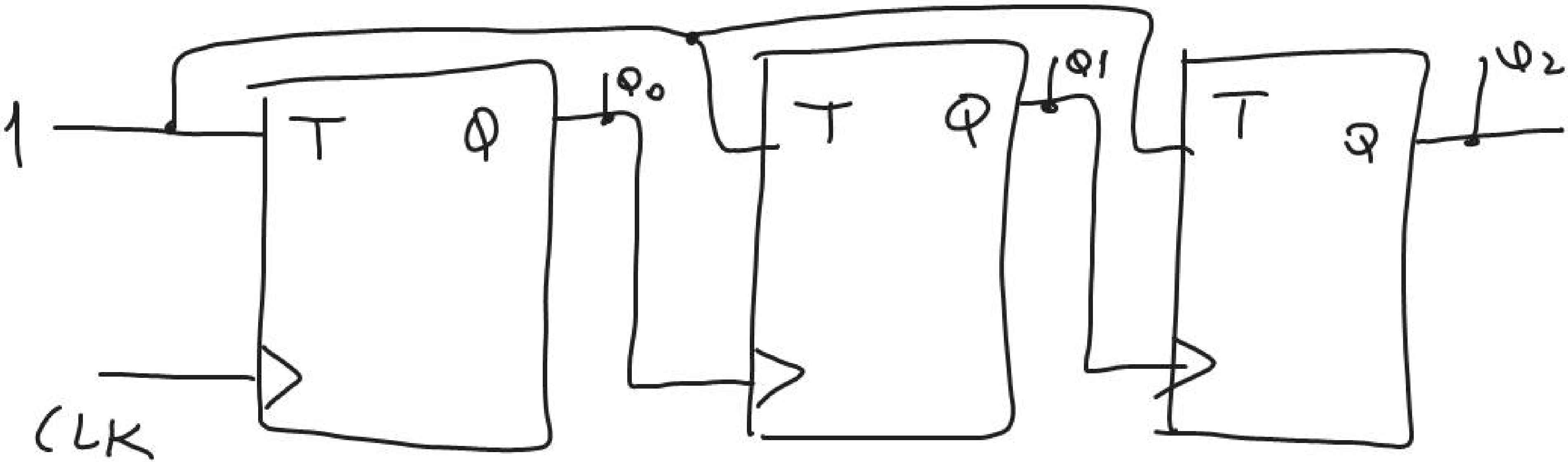
up-counter with T flip flops

T	Q_n	
0	Q_{n-1}	Holds
1	$\overline{Q_{n-1}}$	Toggles



Ripple. Accumulation of propagation times of CLK signal

Count-down Ripple ~~Register~~ Counter



SYNCHRONOUS COUNTERS

Clock signal is applied at the same time to all registers. flip-flops

They do not have clock RIPPLE problem.

They can be designed in a regular method.

Present States | next States

Q_2	Q_1	Q_0	T_2	T_1	T_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	1	1	1

$T_0 = 1$

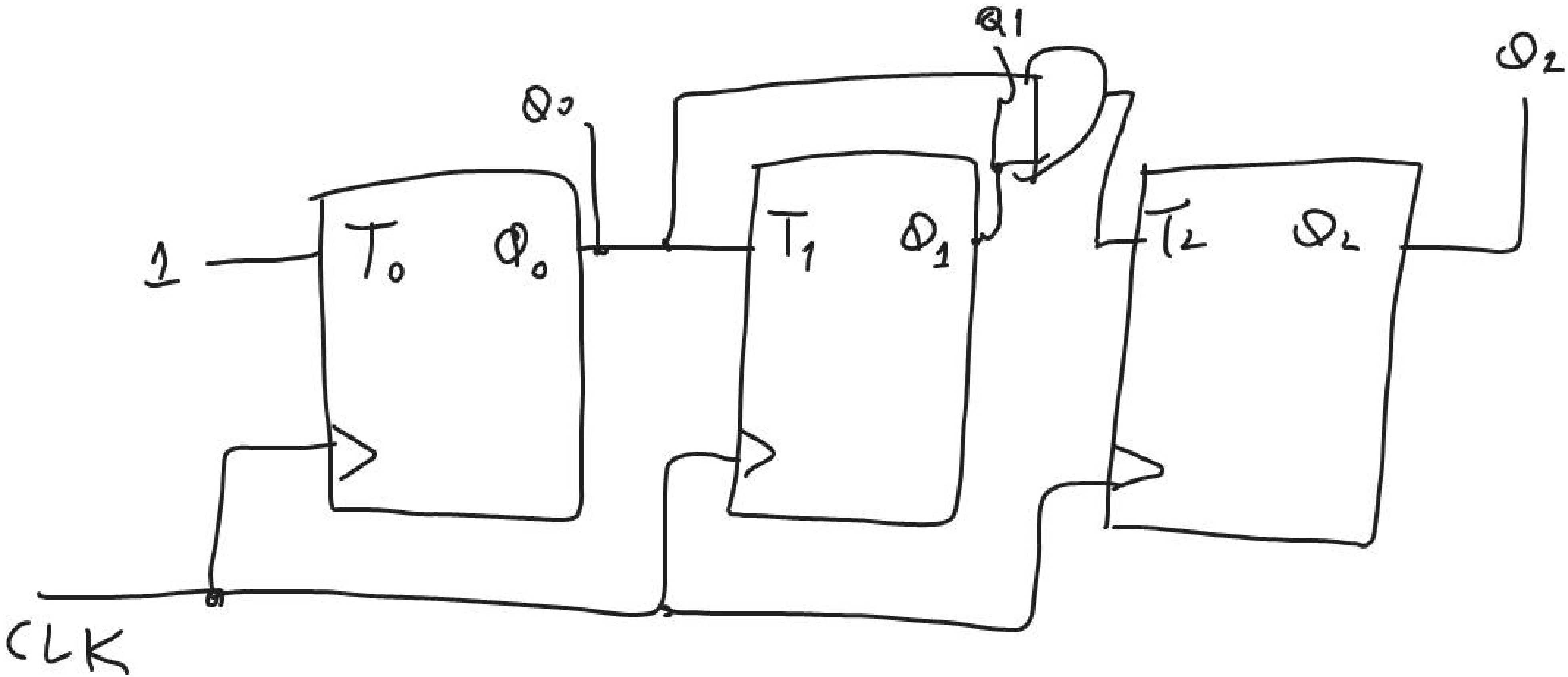
T_1

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$T_2 = Q_1 \cdot Q_0$

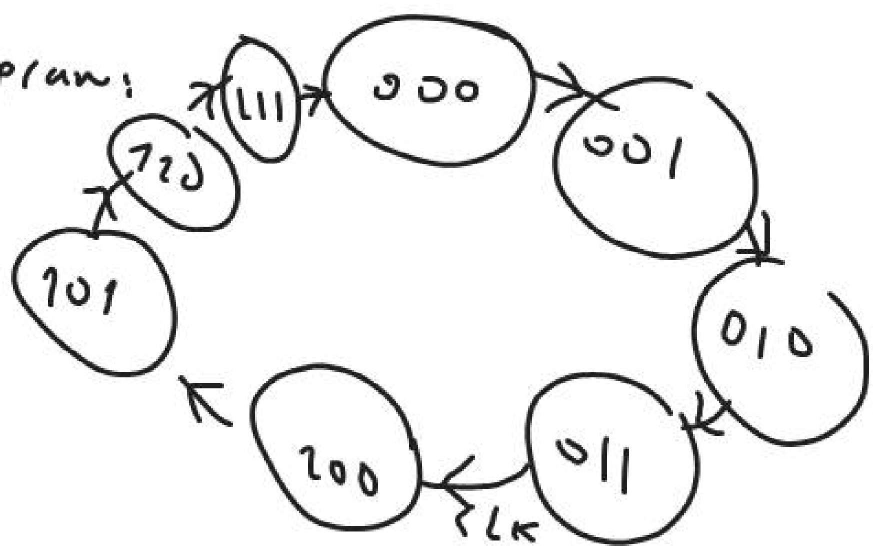
$T_1 = Q_0$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	0	1	0
1	0	0	1	0

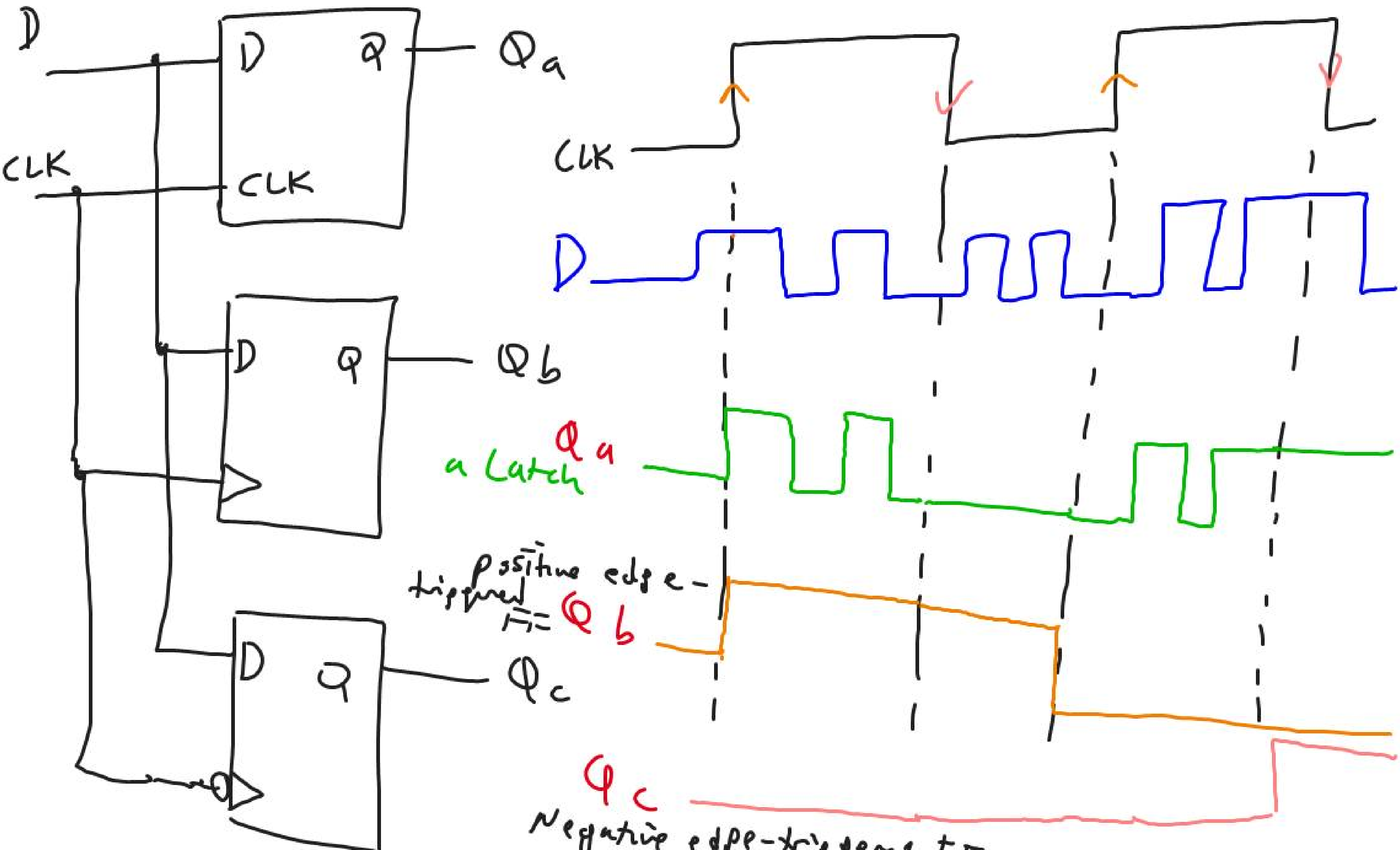


It is a Finite State Machine (FSM)

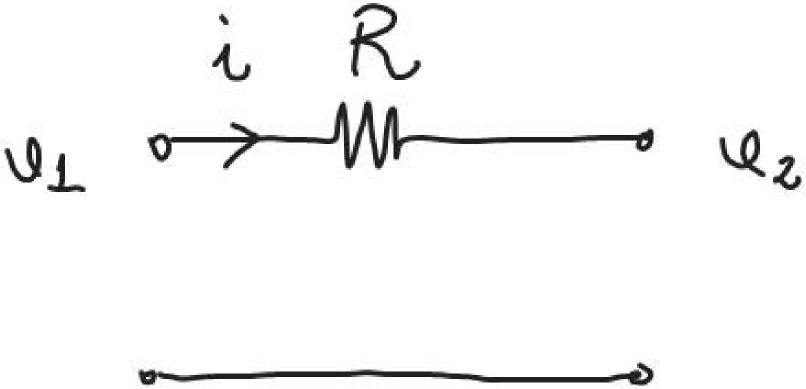
State Diagram:



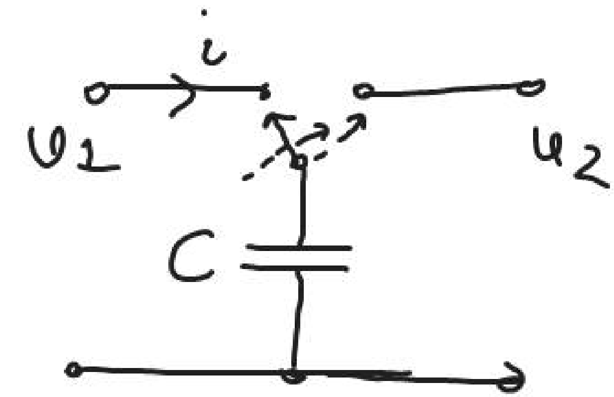
Example:


D
CLK
D
Q
CLK
Qa
D
Q
Qb
D
Q
Qc
CLK
D
Qa
a Latch
positive edge-triggered FF
Qb
Qc
Negative edge-triggered FF

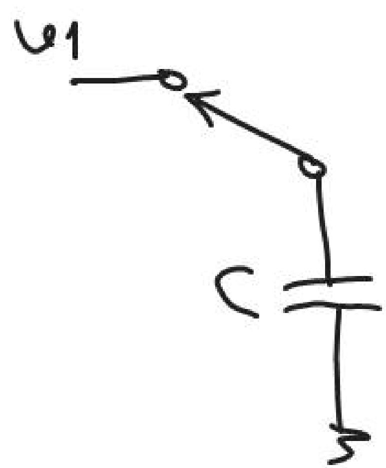
A switched Capacitor acting as a Resistor



$\overset{?}{\equiv}$



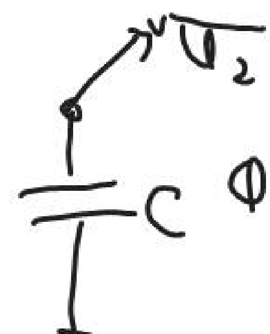
$$Q = CV$$



$$Q_1 = C \cdot v_1$$

The charge transferred by the capacitor in 1 period of switching

$$Q = C(v_1 - v_2)$$



$$Q_2 = C \cdot v_2$$

$$Q_1 - Q_2 = C(v_1 - v_2)$$

$$i = \frac{dq}{dt} \doteq \frac{\Delta q}{\Delta t} = \frac{C(v_1 - v_2)}{T}$$

switching period

$$i = \frac{v_1 - v_2}{R}$$

when we have the resistor

$$i = \frac{C(v_1 - v_2)}{T}$$

when we have the switched capacitor

$$\frac{\cancel{v_1 - v_2}}{R} = \frac{C\cancel{(v_1 - v_2)}}{T}$$

$$\boxed{R = \frac{T}{C}}$$

if we select the C and T properly we obtain the required resistance

In integrated circuits → manufacturing transistors and capacitors are preffered to manufacturing R and L.