WIRES

31.12.2010

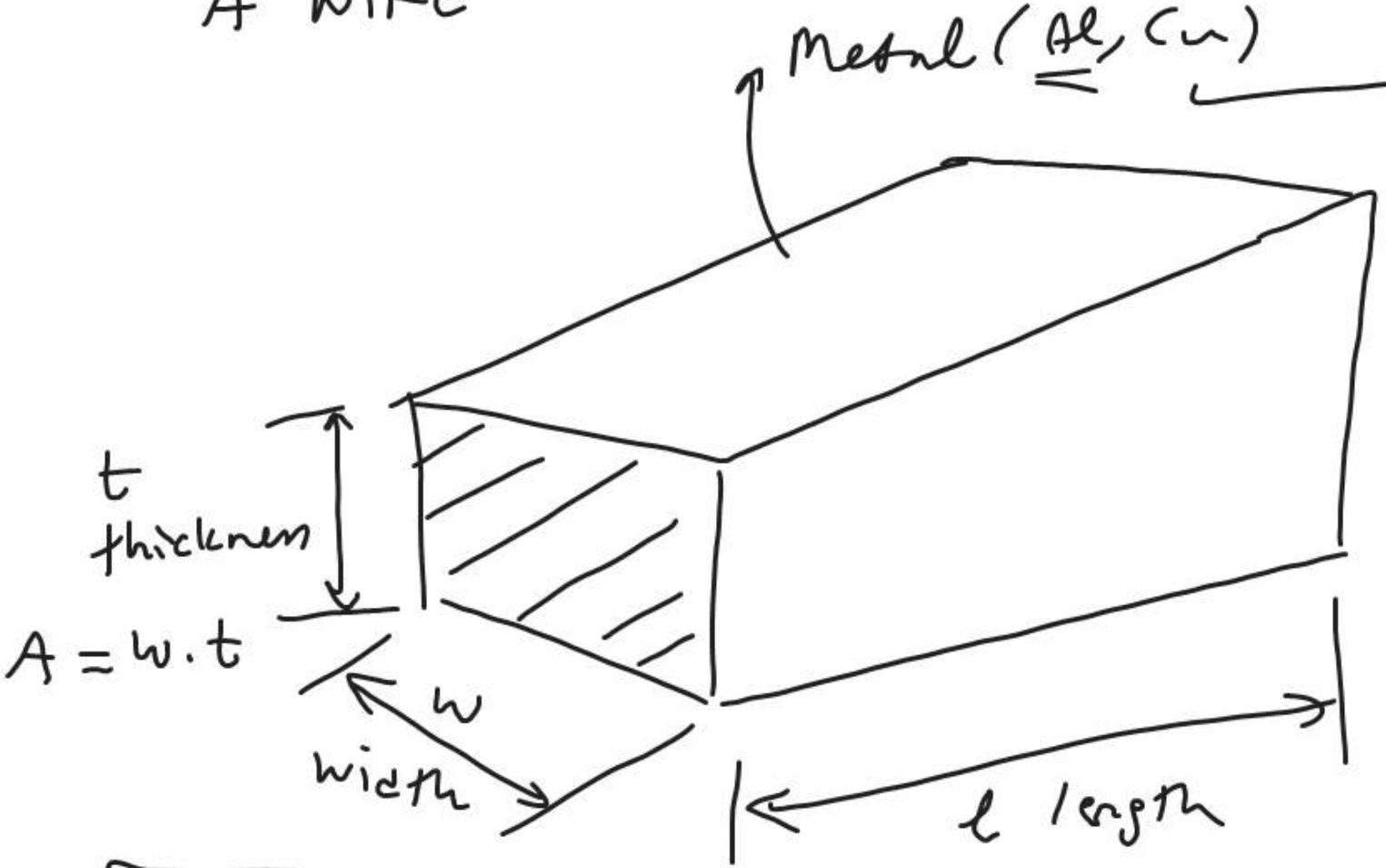
- wires in CMOS technology
- long wires getting slower on time if a DC current passes which causes the migration of metal atoms
- wire delay is a function of wire resistance and wire capacitance

$$\tau = RC$$

Ex IBM CMOS 7 Process

6 layers of Copper (Cu) wiring
1 layer of Tungsten interconnect

A WIRE



The thickness of the wire is constant through the die.

$$R = \rho \cdot \frac{l}{A} \quad = (\Omega\text{-cm}) \frac{\text{cm}}{\text{cm}^2}$$

$$R = \rho \cdot \frac{l}{w.t}$$

$$R = \left(\frac{\rho}{t}\right)\frac{l}{w} = \Omega \cdot \underbrace{\text{a number}}$$

$\frac{\rho}{t}$ ↓ constant for a wire of certain metal and thickness.

number of squares in $\frac{l}{w}$

$$\frac{\rho}{t} = \frac{\Omega - \text{cm}}{\text{cm}} = \Omega$$

$$\frac{l}{w} = \frac{\text{cm}}{\text{cm}} = \text{unitless} \rightarrow \text{a number}$$

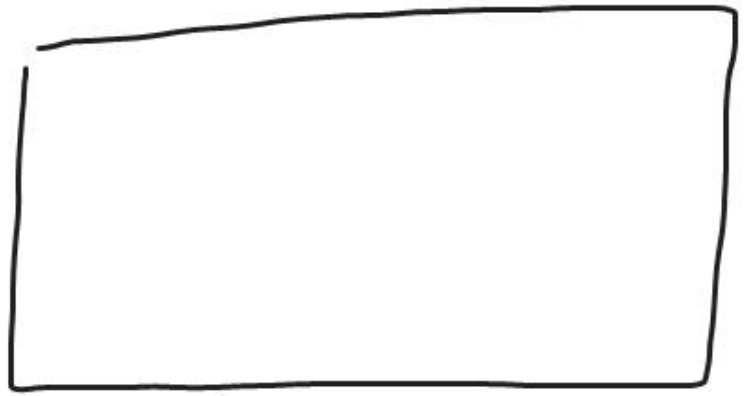
ext

$l = 1\text{mm}$

$w = 0.5\mu\text{m}$

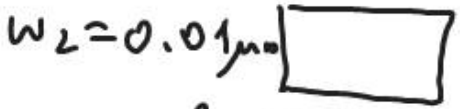
$0.5\mu\text{m}$

$$\frac{l}{w} = \frac{1\times10^{-3}}{0.5\times10^{-6}} = 2000 \text{ squares}$$



$\frac{l_1}{w_1} = \frac{100\mu m}{1\mu m} = 100$ squares

$R_1 = X\Omega \cdot 100$ → withstands more power



$\frac{l_2}{w_2} = \frac{1\mu m}{0.01\mu m} = 100$ squares

$R_2 = X\Omega \cdot 100$

same resistance

same aspect ratio $\left(\frac{l}{w}\right)$ will give the same R (if they are of the same metal)

ρ (Ω-m)	
2.8×10^{-8}	Al
1.7×10^{-8}	Cu
1.6×10^{-8}	Ag

TSMC

0.18μm 6 Al metal layers

M1-5 $0.08\,\Omega$/square $\left(\frac{\rho}{t}\right)$

M6 $0.03\,\Omega$/square

If we have a $1\mu m = l$, and $w = 0.2\mu m$ wire of M5

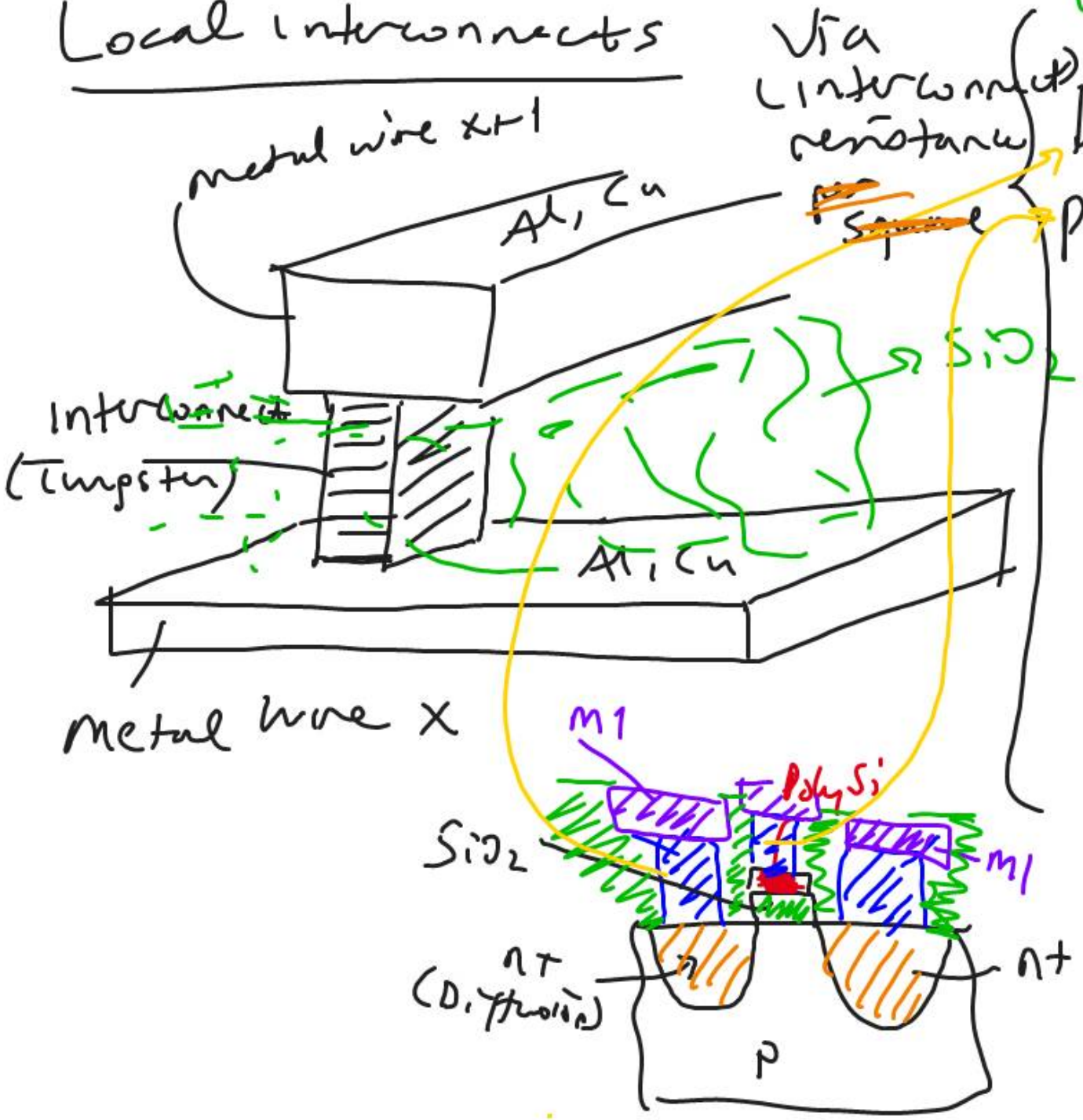
$$R = \frac{0.08\,\Omega}{\text{square}} \times \left(\frac{l}{w}\right) = \frac{0.08\,\Omega}{\square} \times 5\square$$

$$R = 0.4\,\Omega$$

$l = \frac{1\mu m}{0.2\mu m}$

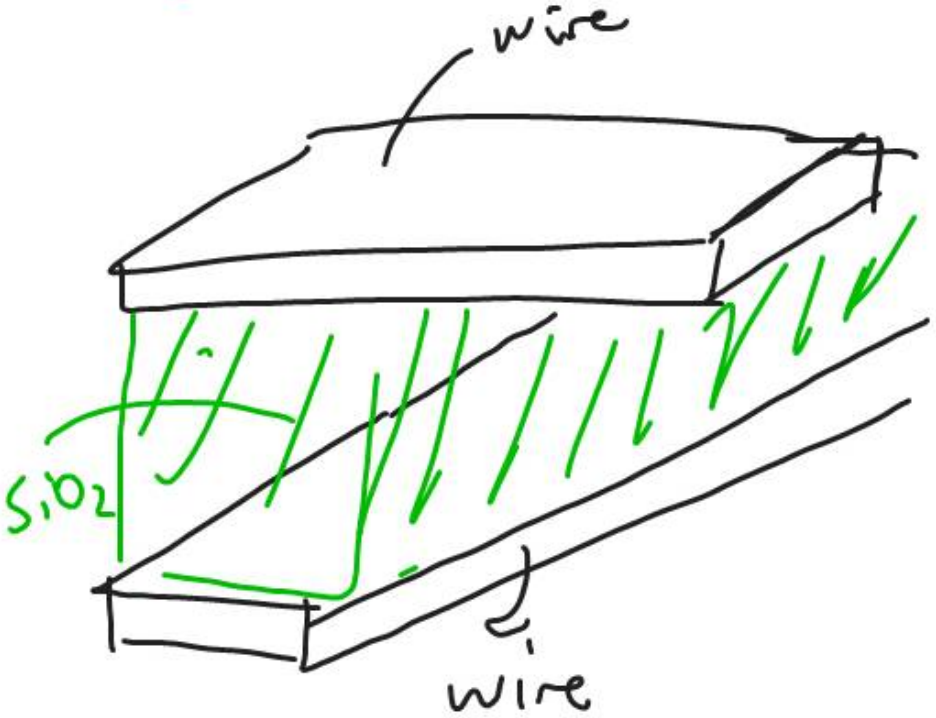
Local interconnects

TSMC 0.18μm 6 Al



Diff – M1:	11 Ω
Poly – M1:	10.4 Ω
M2 – M1	4.5 Ω
M3 – M1	9.5 Ω
M4 – M1	15 Ω
M5 – M1	19.6 Ω
M6 – M1	21.8 Ω

WIRE CAPACITANCE



ϵ = permittivity of the material

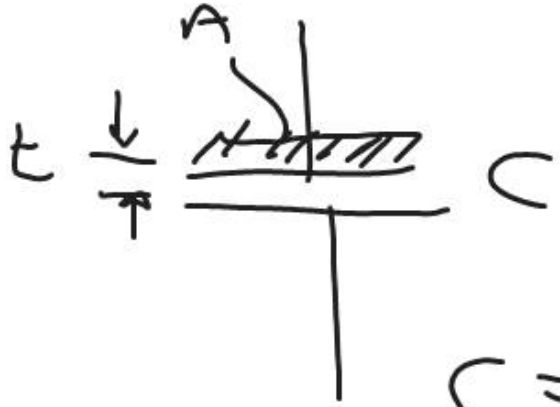
$\epsilon = \epsilon_0 \cdot \epsilon_r$ Absolute permittivity

ϵ_0 = permittivity (F/m)

ϵ_r = relative permittivity

	ϵ_r
SiO_2	3.9
SiOF	3.1
Silk Polymer	2.6
Si	11.7

$\epsilon_r = 1$ for vacuum ~ air



$$C = \epsilon \cdot \frac{A}{t}$$

$$C = \epsilon \frac{A}{t} = \epsilon \frac{w \cdot l}{t}$$

$t \rightarrow$ thickness of the insulator (e.g. SiO_2) between the metal layers

$$\frac{C}{l} = \epsilon \left(\frac{w}{t}\right)$$

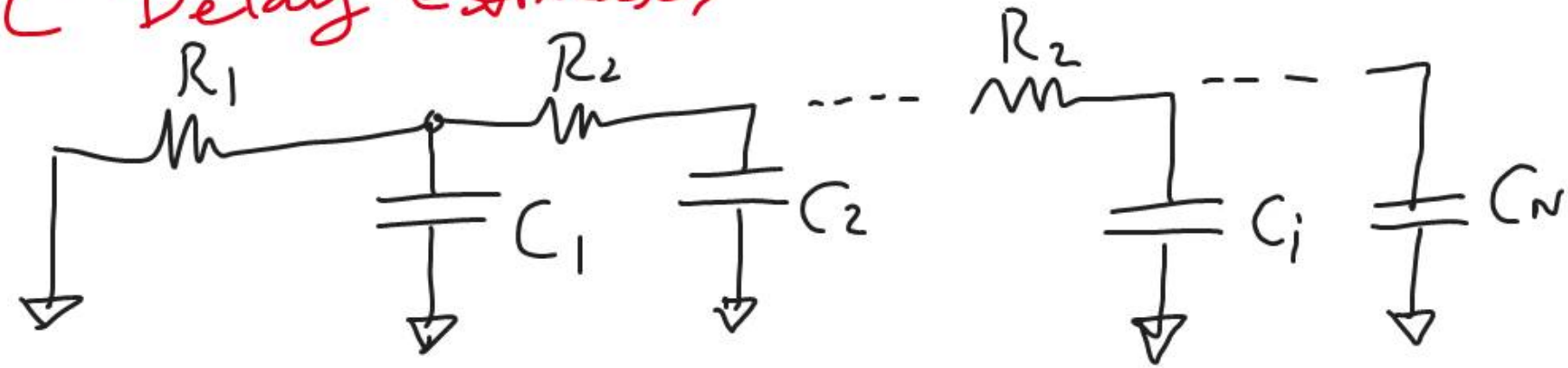
$w \cdot l = A =$ effective area of the metal wires overlapping

- 100 fF/mm ⇒

femto $= 10^{-15}$

- 160 fF/mm

RC Delay Estimates

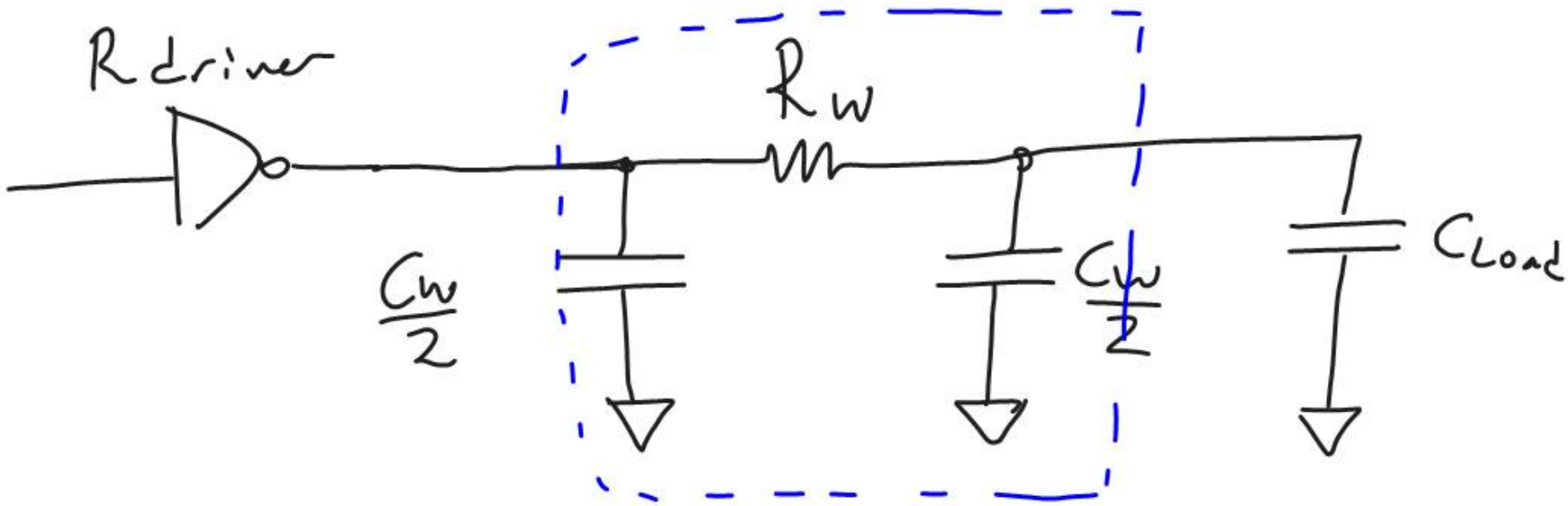


Panfield - Rubinstein Model estimates

$$DELAY \simeq \sum_{i=1}^{N} \left(\sum_{j=1}^{i} R_j \right) C_i$$

$$N=3 \quad = R_1 C_1 + (R_1+R_2) C_2 + (R_1+R_2+R_3) C_3$$

Simple Lumped-π model



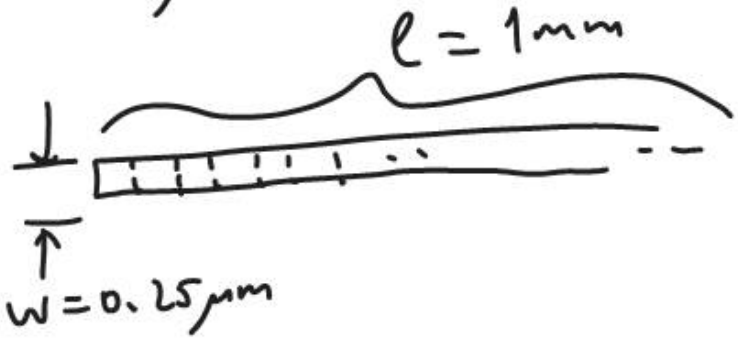
$$DELAY = R_{driver} \times \frac{C_w}{2} + \left(R_{driver} + R_w\right) \times \left(\frac{C_w}{2} + C_{load}\right)$$

Example: 0.18μm TSMC, 5x minimum inverter with effective resistance of 3kΩ, FO4 load (25fF)

$$Delay = R_{driver} \times C_{Load} = 3k\Omega \times 25fF = 75ps$$

Now add 1mm M_1 wire, 0.25μm wide

$$\rho_{m1-m5} = 0.08\,\Omega/\square$$



$$\square = \frac{l}{w} = \frac{1mm}{0.25\mu m} = \frac{1mm}{0.25 \times 10^{-3}mm} = \frac{10^3}{0.25} = 4000\,\square$$

$$R_w' = 4000\,\square \times 0.08\,\Omega/\square = 320\Omega$$

$$R_{vias} = 22\Omega$$

$R_w = R_w' + R_{via} = 320 + 22 = 342\,\Omega$

$C_w = 160\,fF$ (remember $\frac{C}{l} = 160\,fF/mm$)

$l = 1\,mm$

$C = 160\,\frac{fF}{mm} \times 1\,mm$

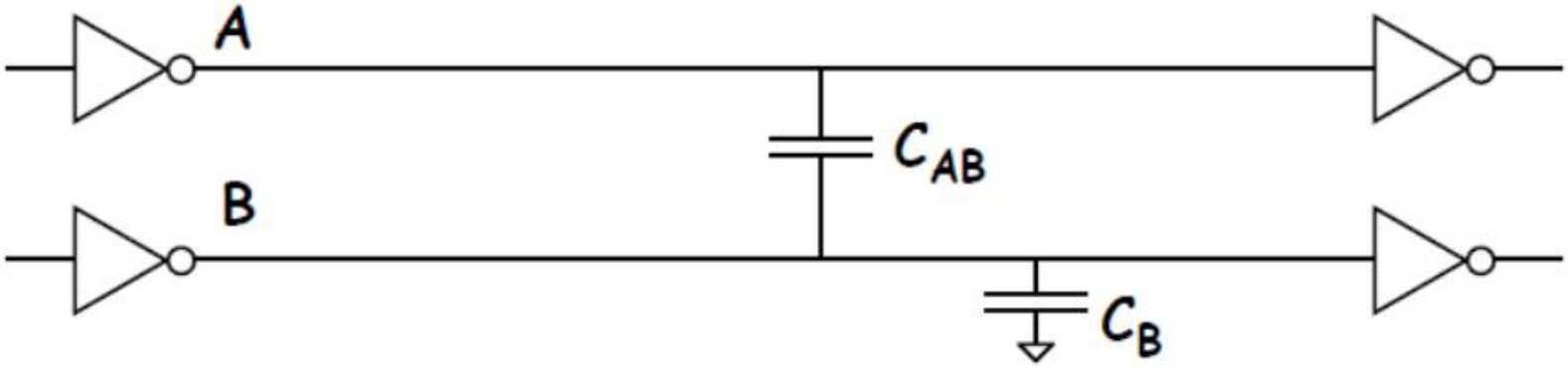
$\boxed{C_w = 160\,fF}$

$Delay = R_{driver} \times \frac{C_w}{2} + (R_{driver} + R_w)\left(\frac{C_w}{2} + C_{load}\right)$

$= 3k\Omega \times 80fF + (3k\Omega + 342\,\Omega)(80fF + 25ff)$

$Delay = 591\,ps \cong 0.59\,ns$

Coupling Capacitances

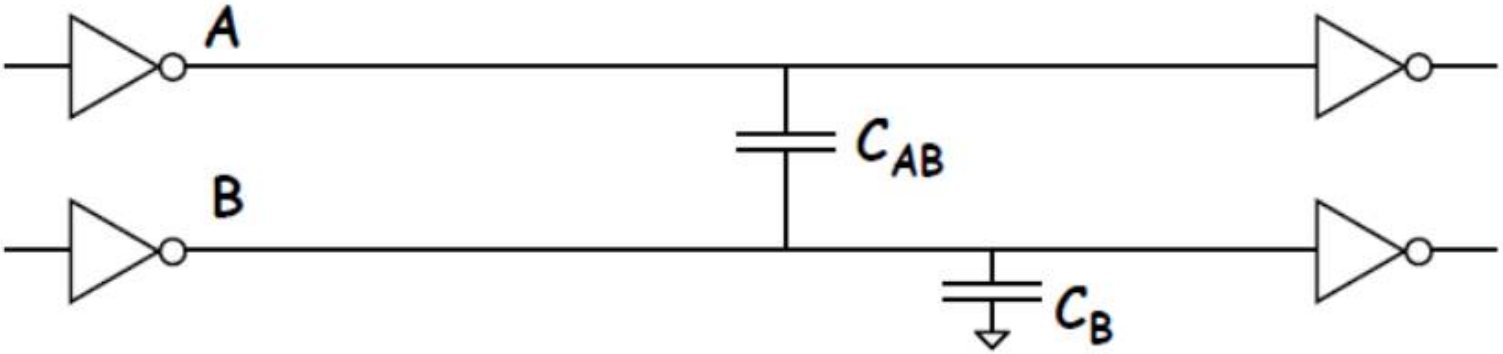


- Most capacitance is to neighboring wires
- If A switches, injects voltage noise on B
  - magnitude depends on capacitive divider formed:

$$C_{AB}/(C_{AB}+C_B)$$

- If A switches in opposite direction while B switches, coupling capacitance effectively doubles – Miller effect
- If A switches in same direction while B switches, coupling capacitance disappears
- These effects can lead to large variance in possible delay of B driver, possibly factor of 5 or 6 between best and worst case

Fixing Coupling Problems



- Avoid placing simultaneously switching signals next to each other for long parallel runs
- Reroute signals which will be quiet during switching inbetween simultaneous switching signals
- Route signals close to power rails to provide capacitance ballast
- Tough problem to solve – moving one wire can introduce new problems
  - "timing closure" causes many real-world schedule slips