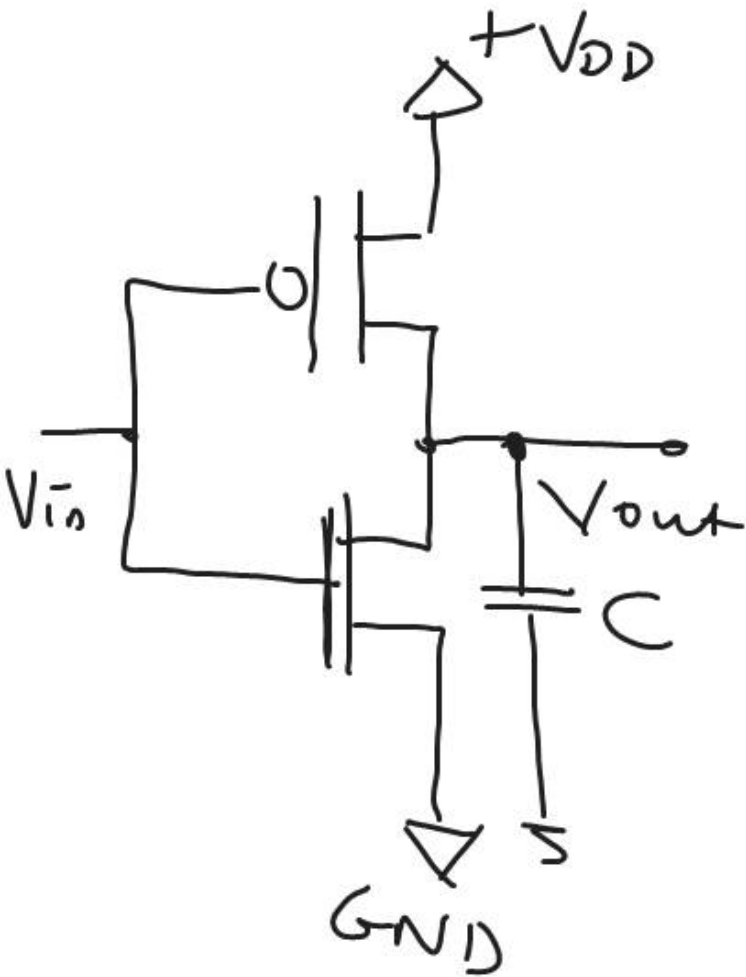


POWER

07.01.2011

©

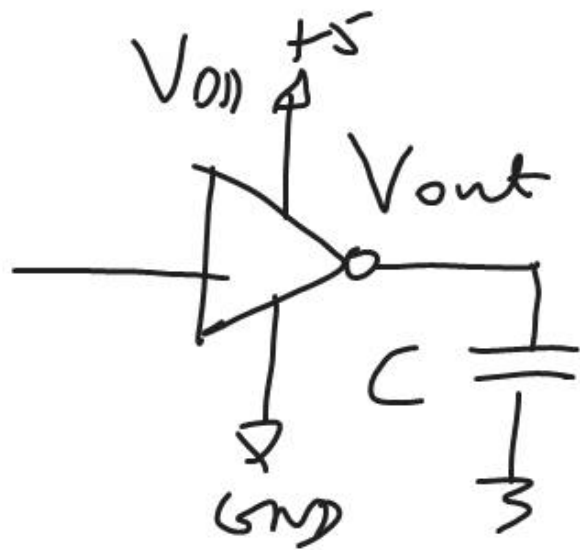


We have limited energy in battery (for mobile devices)

We should consume the lowest amount of power.

Power is the rate of use of energy.

$$Power = \frac{Energy}{Time} = Energy \times Frequency$$



energy is
drawn from the
battery during
a 0-1 transition

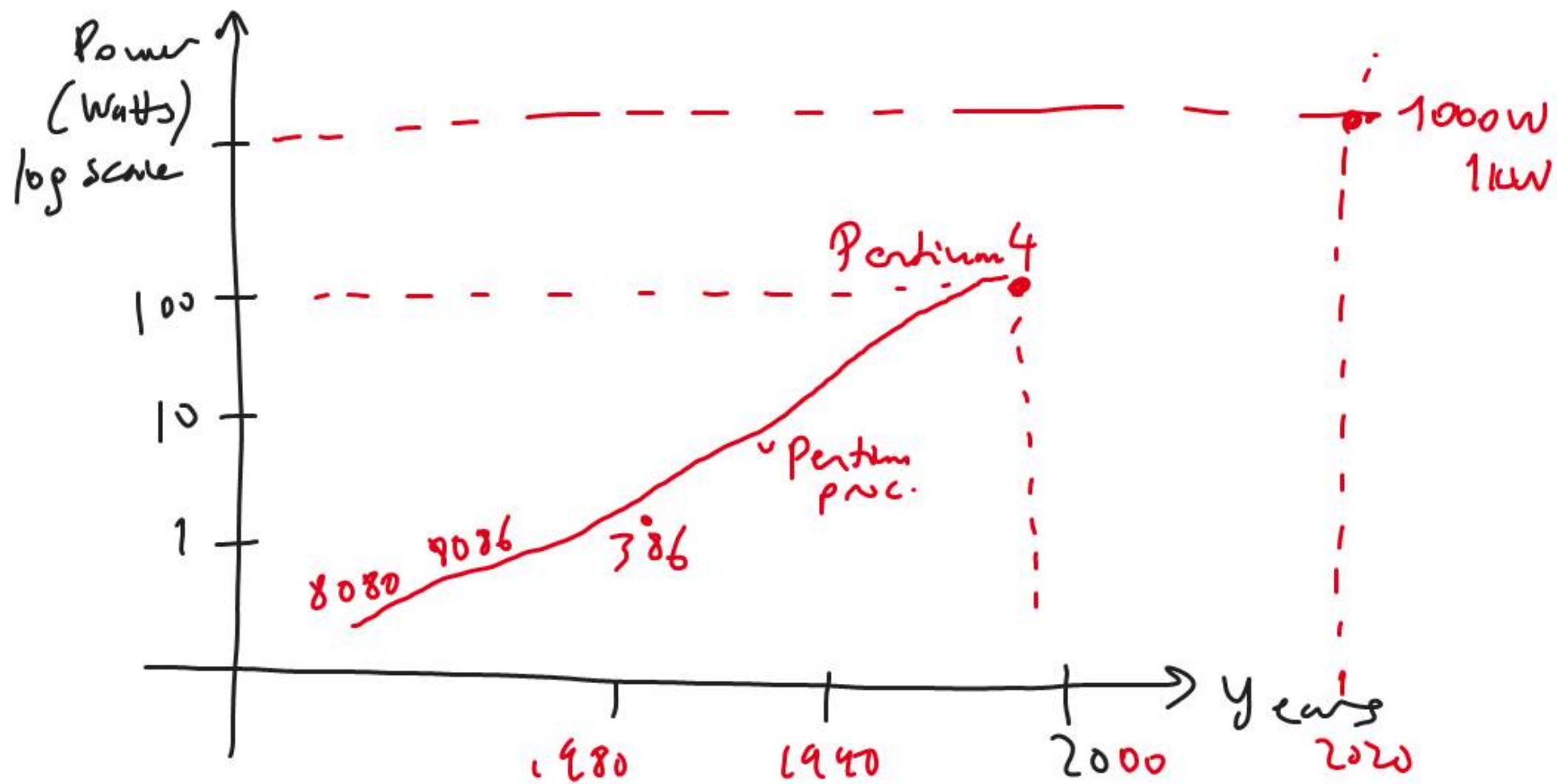
$$E = CV_{DD}^2$$

The stored energy
in the Capacitor -
is consumed
as heat on the
pull-down transistor.

$$\frac{1}{2} CV_{DD}^2$$

$\frac{1}{2} CV_{DD}^2$ is stored in
the C

$E_{consumed} = \frac{1}{2} CV_{DD}^2$
+ as heat in charging



Internet data center has ~ 8000 servers $\Rightarrow$ 2 MW
 25% Power is added to cool (take the heat out) the devices.

ENVIRONMENTAL CONCERN!

In 2010 ~ 2 Billion PCs

$$2 \times 10^9 \cancel{\text{PCs}} \times 100 \text{ W} / \cancel{\text{PC}} = 200 \times 10^9 \text{ W} = \underline{200 \text{ GW}}$$

1 Hoover Dam in Las Vegas $\rightarrow$ 2.5 GW

For only PCs This much of power is needed.

A very big ENVIRONMENTAL ISSUE!

We should reduce the Power Consumption ~~xxx~~

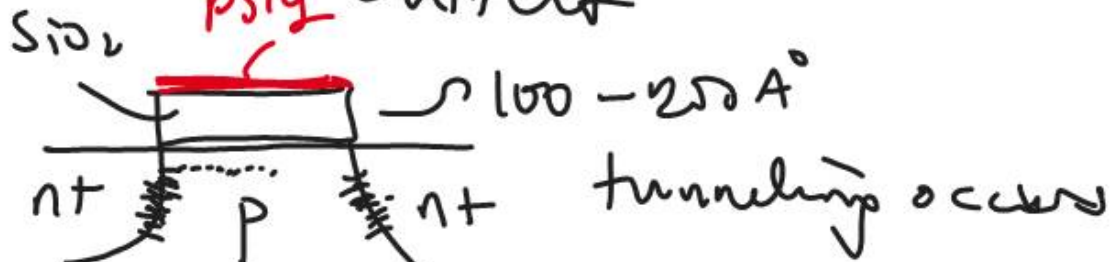
POWER DISSIPATION

1. Charging & discharging the capacitor during switching ($\frac{1}{2} CV^2$)

2. Short circuit current

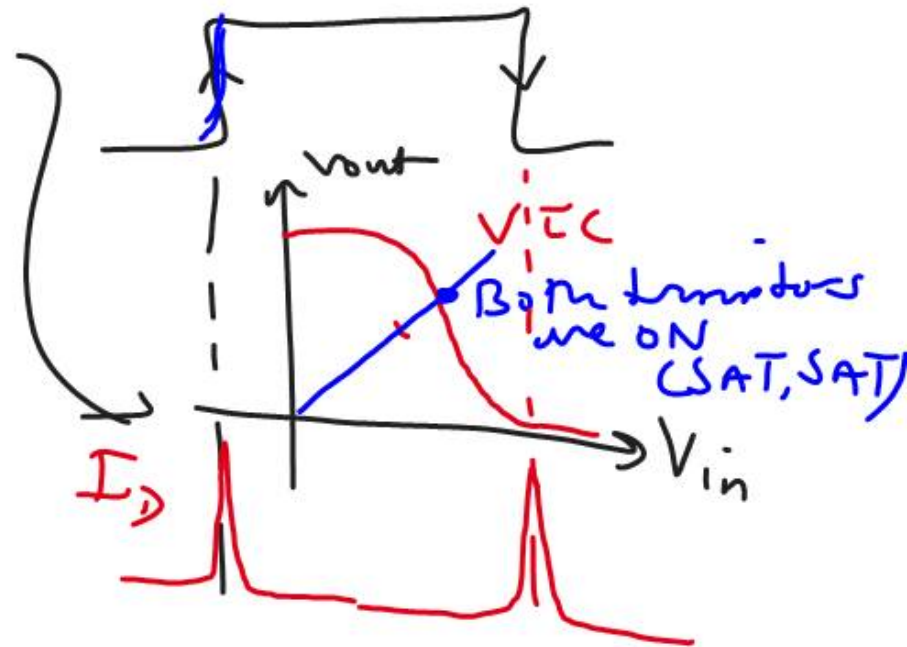
3. Gate tunneling current

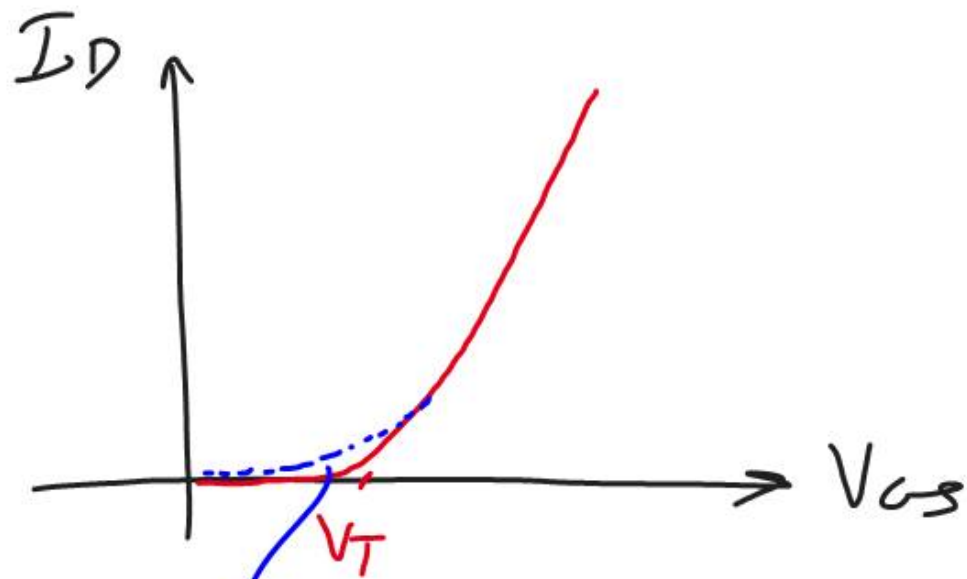
poly current



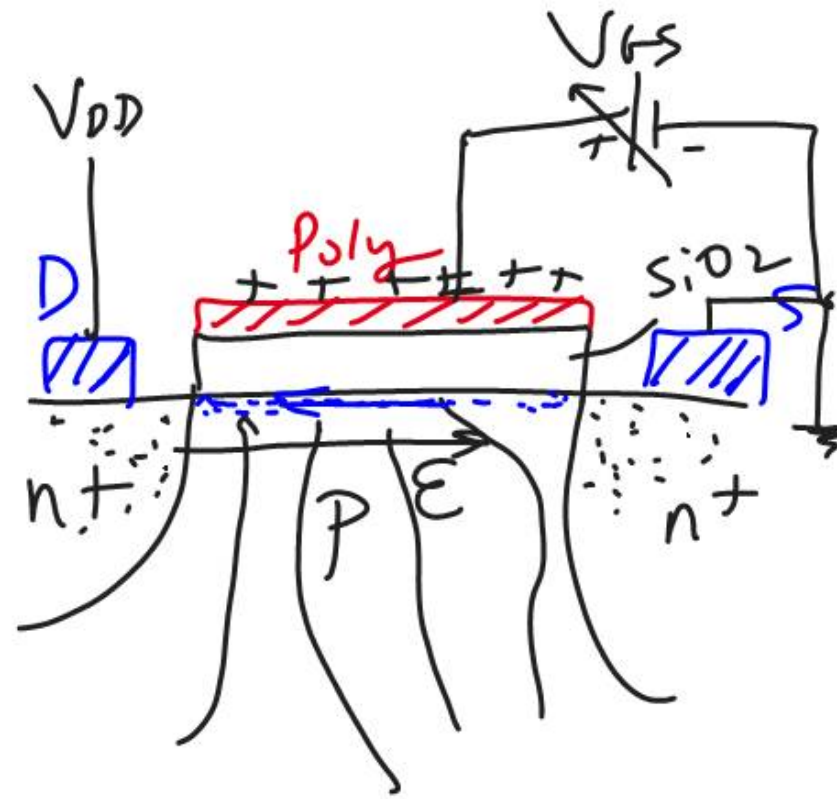
4. Drain and Source Reverse Diode Leakages

5. Subthreshold (V_T) Leakage





Subthreshold leakage
of I_D with V_{GS}



SWITCHING POWER

$$\text{Power} = \text{Activity} \times \text{frequency} \times \left(\frac{1}{2} C V_{DD}^2 + \right. \\ \left. \frac{V_{DD} \bar{I}_{SC}}{V_{DD}} + V_{DD} \bar{I}_{\text{subthreshold}} + \right. \\ \left. V_{DD} \bar{I}_{\text{diode}} + V_{DD} \bar{I}_{\text{tunneling gate}} \right)$$

Activity is the # of circuits switched at that frequency

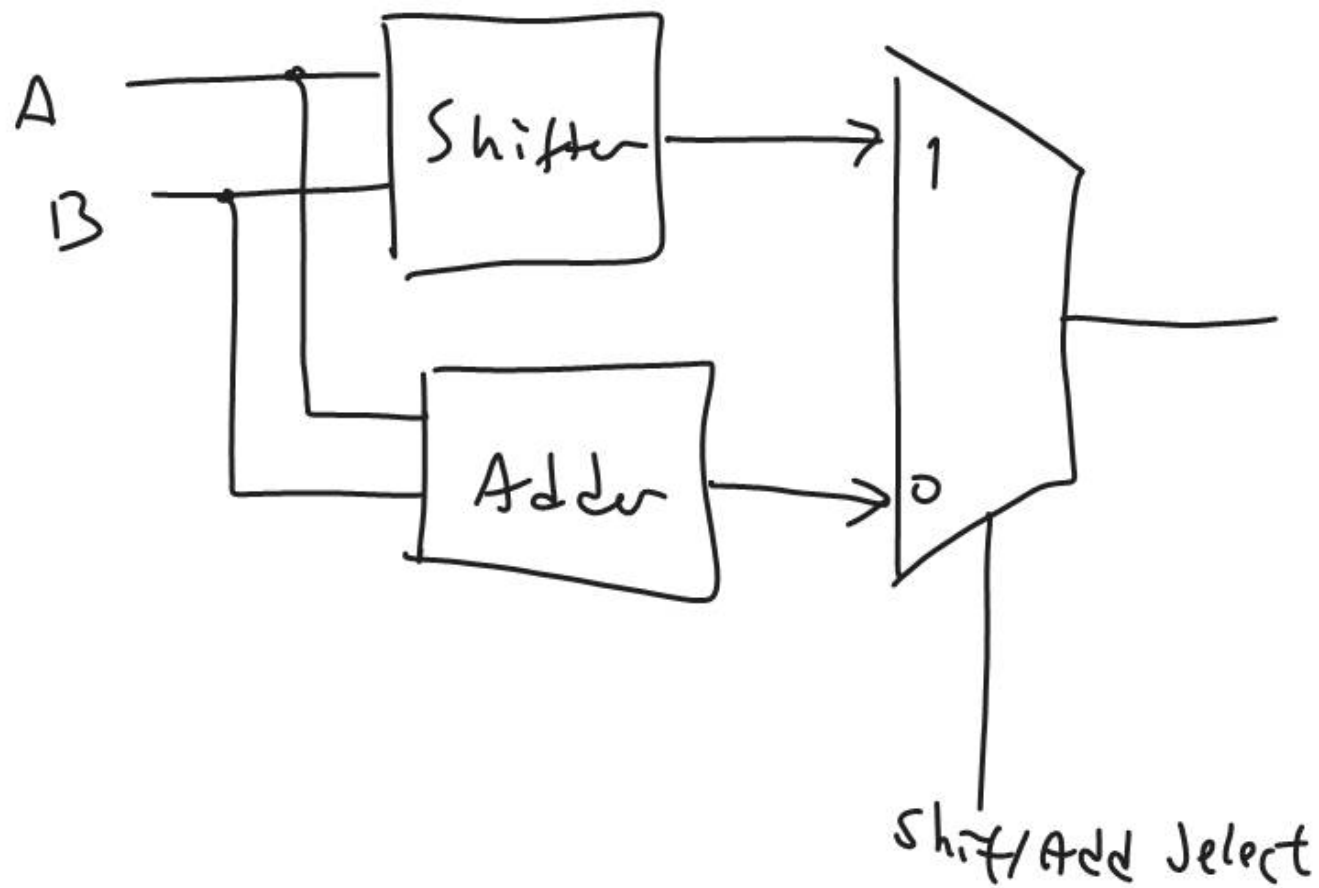
$$\text{Power} \cong \text{Activity} \times \frac{1}{2} C V^2 \times \text{Frequency}$$

To minimise the power dissipation:

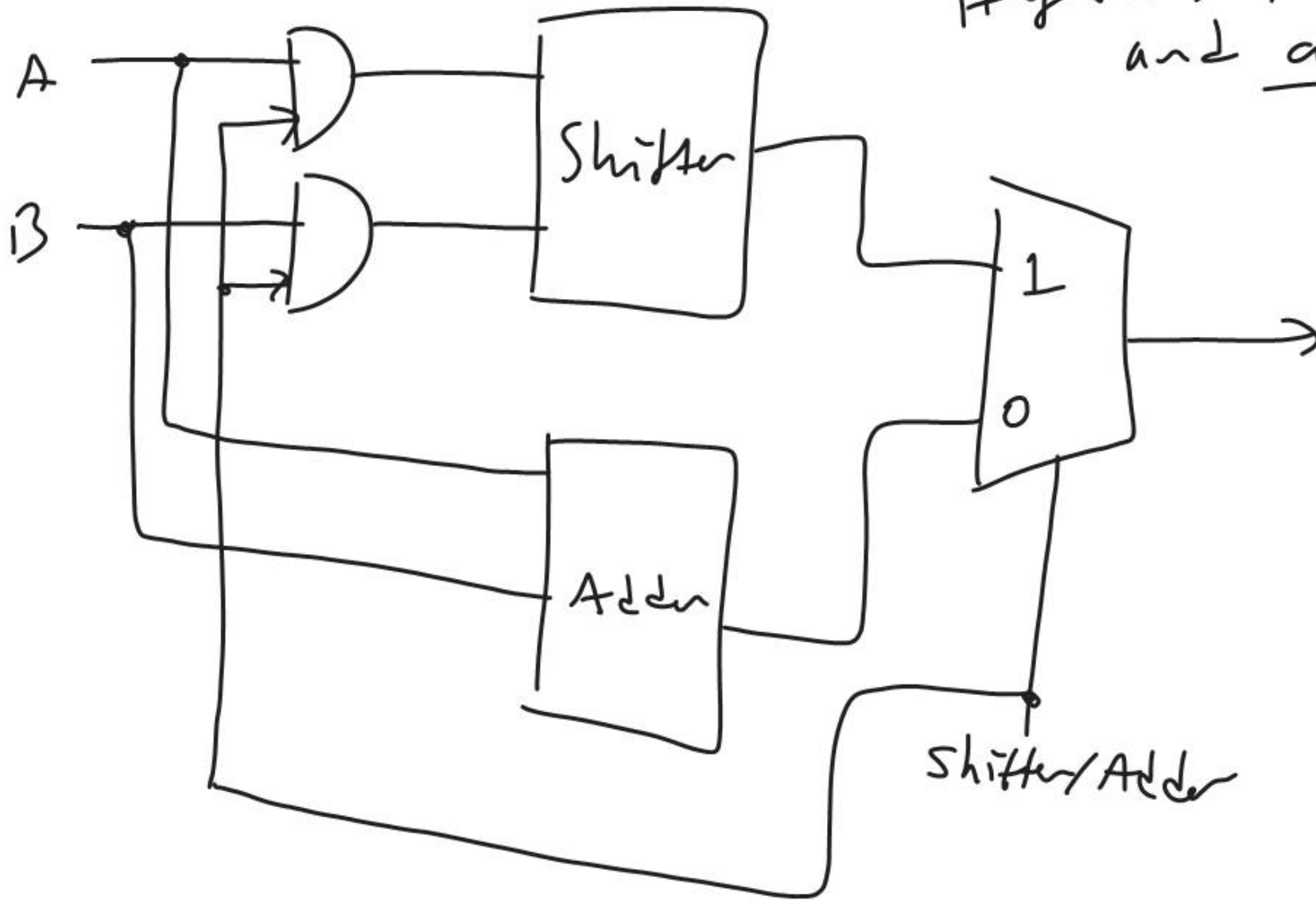
- 1 - reduce ACTIVITY
- 2 - reduce switching capacitance C
- 3 - reduce supply voltage (V_{DD})
- 4 - reduce frequency

1-Reduce Activity

• Data Gating

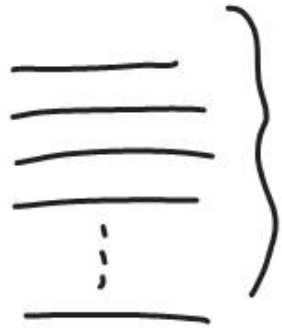


Gating reduces the
of transactions
and activity



Other methods to reduce Activity:

- Bus encodings

 parallel digital signal lines $\Rightarrow$ a Bus

Gray code $\Rightarrow$ reduces transitions (switching)

$\begin{matrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \\ & & \vdots \\ & & \vdots \end{matrix}$ $\left. \begin{matrix} \downarrow \\ \downarrow \\ \downarrow \end{matrix} \right\} \begin{matrix} 2 \text{ changes in} \\ 1 \text{ count} \end{matrix}$

$\begin{matrix} 0 & 0 & 1 & \rightarrow 1_{10} \\ 0 & 1 & 1 & \rightarrow 2_{10} \\ 0 & 1 & 0 & \rightarrow 3_{10} \\ 1 & 1 & 0 & \rightarrow 4_{10} \end{matrix}$

• Freeze Don't Cares

1, X, 1, 0, X, 0



Don't care

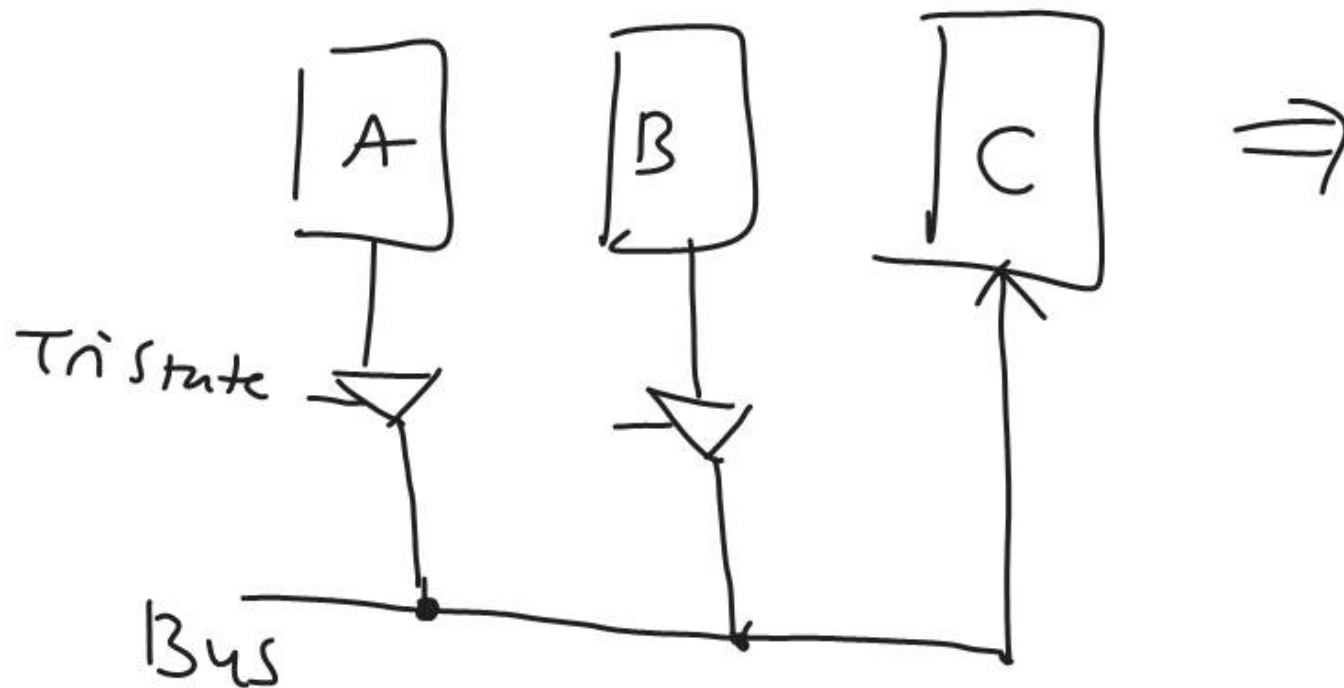
1, X=1, 1, 0, X=0, 0



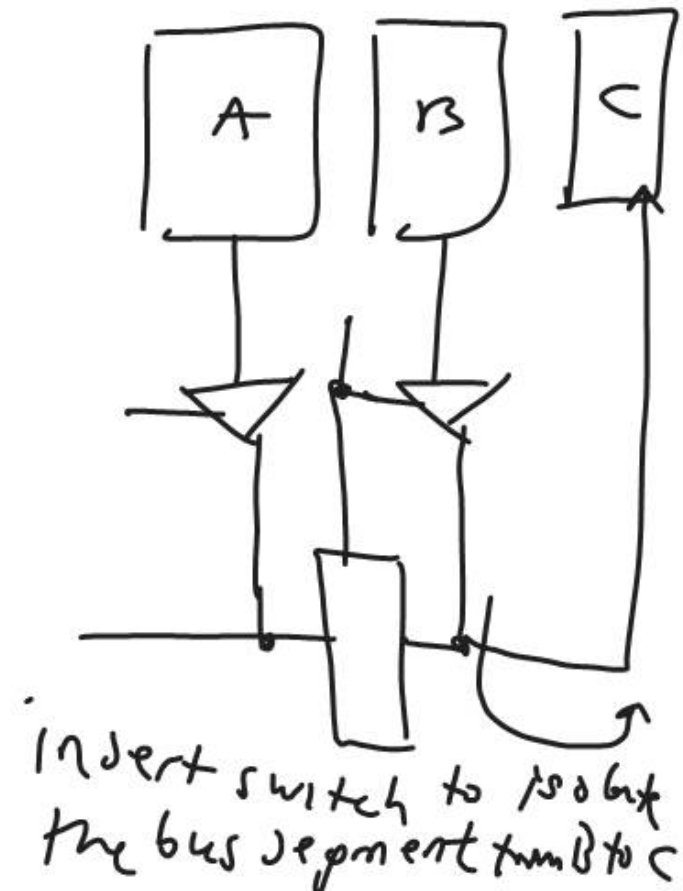
Freeze Don't cares

2 - Reduce CAPACITANCE

- careful transistor sizing
- Tighter layout (good floorplanning)
- Segmented structures



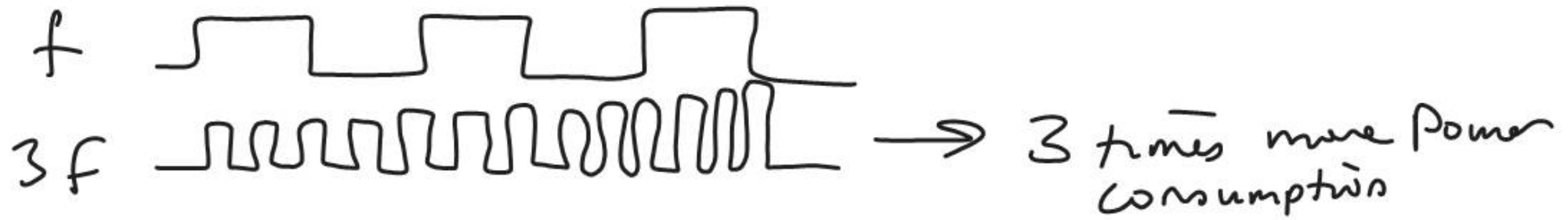
If a signal is routed from B to C



Insert switch to isolate the bus segment from B to C

3-Reducing FREQUENCY

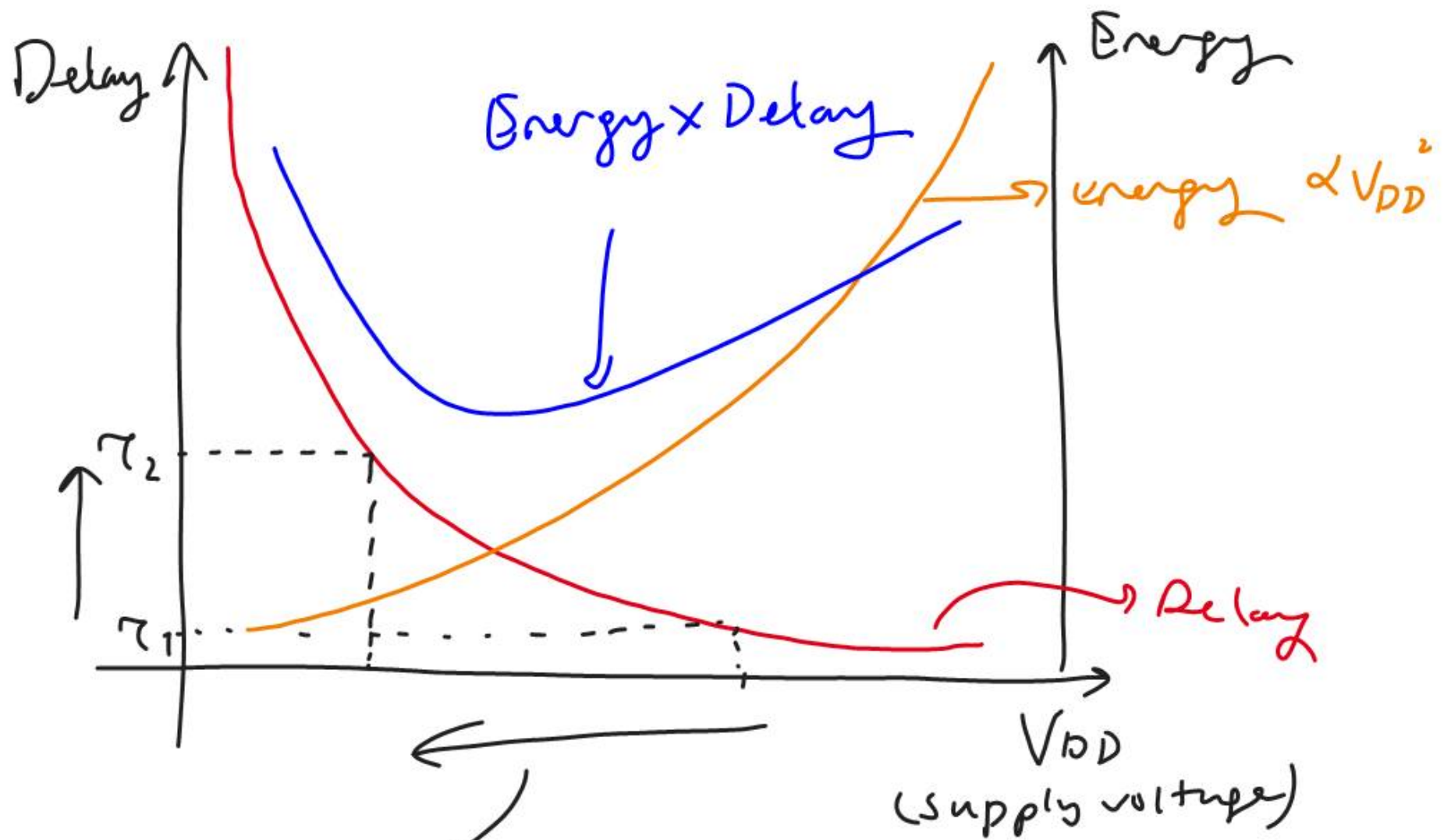
$$P \equiv \text{ACTIVITY} \times \text{frequency} \times \left(\frac{1}{2} C V_{DD}^2\right)$$



4-Reducing the Supply Voltage (V_{DD})

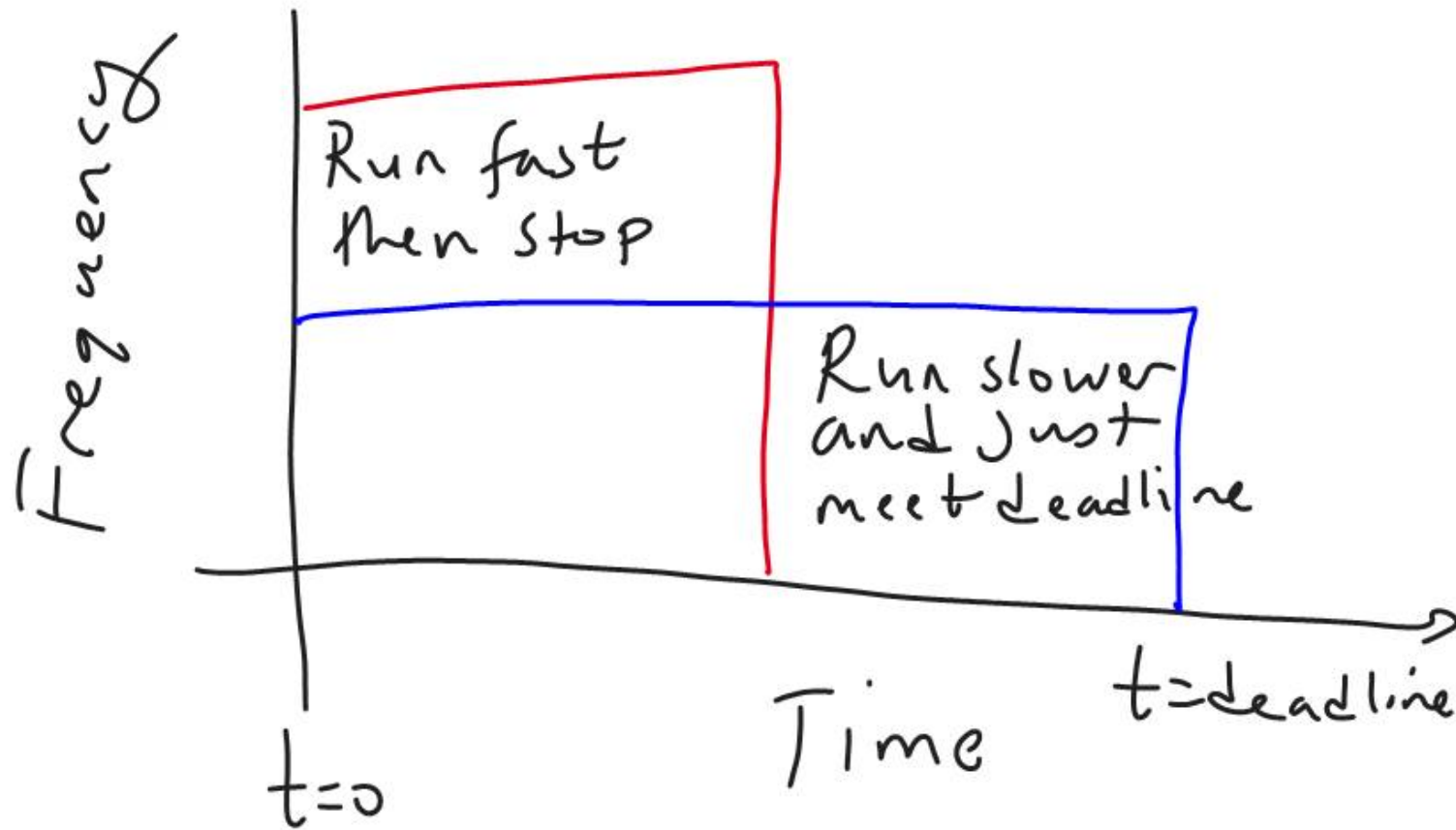
Reducing V_{DD} $\rightarrow$ will affect Power & V_{DD}^2

However reducing V_{DD} should make increasing the delay time a must.



Delay rises sharply when V_{DD} gets small enough

"Just Enough" performance:



Save Energy by reducing frequency and Voltage to minimum necessary

Energy versus delay

