Digital Integrated Circuits (ICs)

08.10.2010

"divide and conquer" approach can be used in digital. Modules (black box) can be used repeatedly to obtain a complex digital system.

This is not possible for an Analog system.

That's why we have digital Very large ICs (VLSI) but not analog VLSIs.

a VLSI has $\gtrsim 10^7$ transistors in a die

a VLSI

ASIC → Application Specific IC

FPGA, CPLD, ..

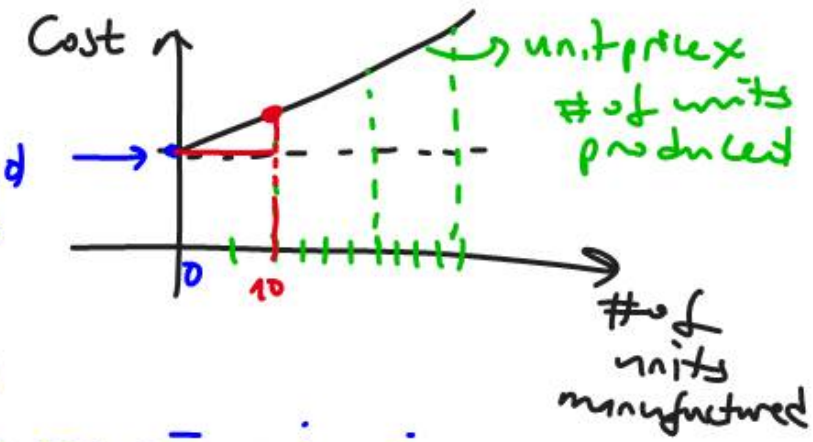
Field Programmable Gate Array

(more generic) reconfigurable

It can be configured by using a hardware Design such as using HDL (hw design language) ⇒ VHDL, Verilog

Cost of IC

fixed cost + variable cost

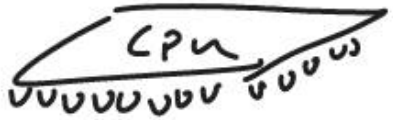


Non-recurring engineering (NRE)

design + prototype test + etc

System

A processor



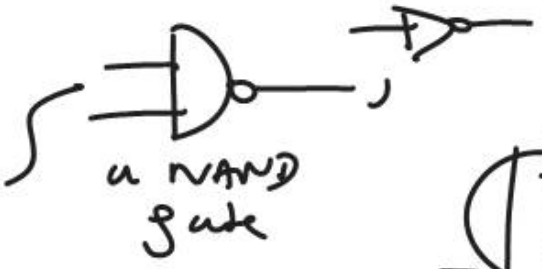
VLSI

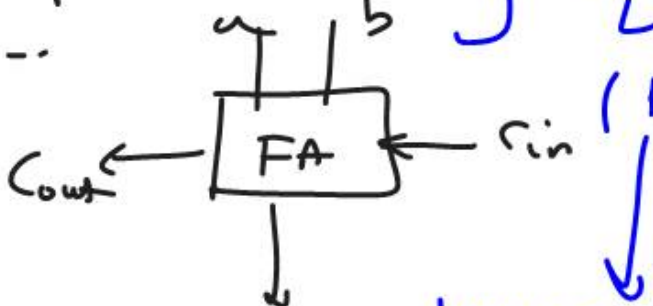
Functional Module

Register, Counter, Multiplier, Adder ...
Multiplexer, Decoder ...

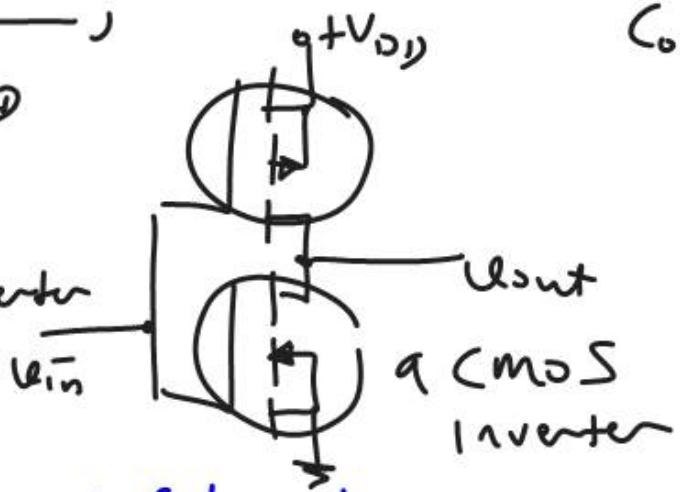
Register Transfer Level (RTL)

Gate





Circuit → An inverter

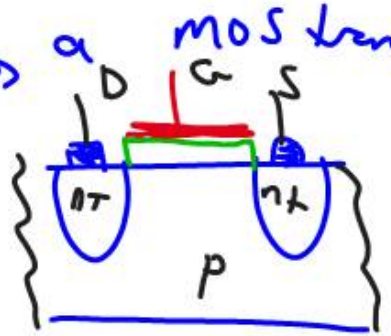


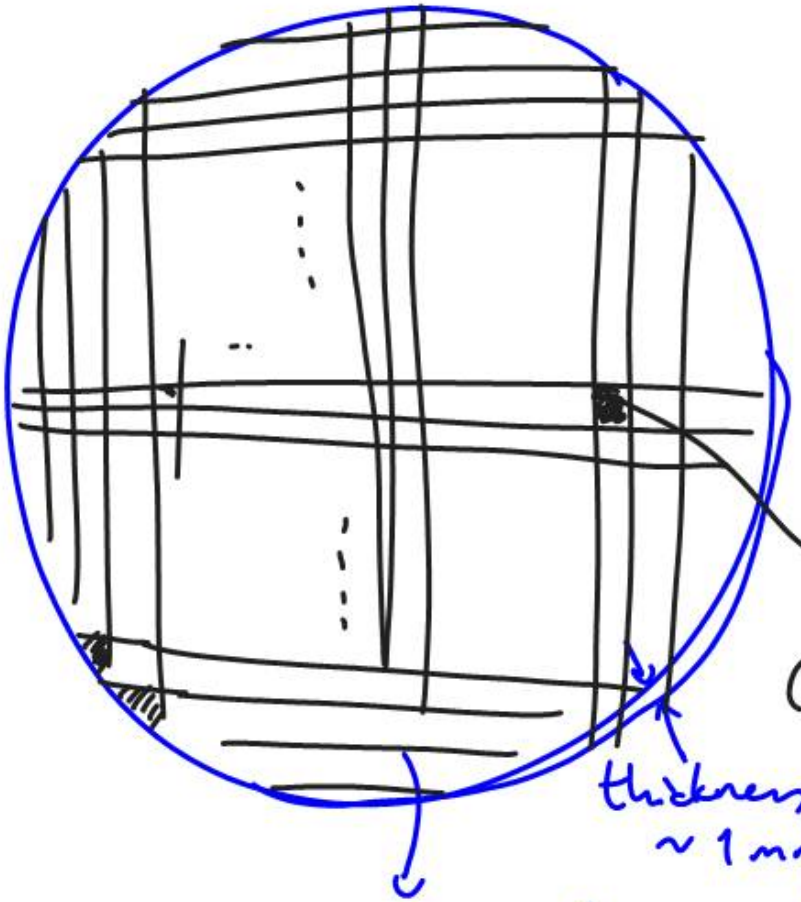
Verilog

HDLs

(VHDL, Verilog)

Device → a MOS transistor





A die
(1.5mm x 1.5mm)
(15mm x 15mm)

thickness
~ 1mm

A wafer (semiconductor, pure crystalline)
(D = 30 cm)

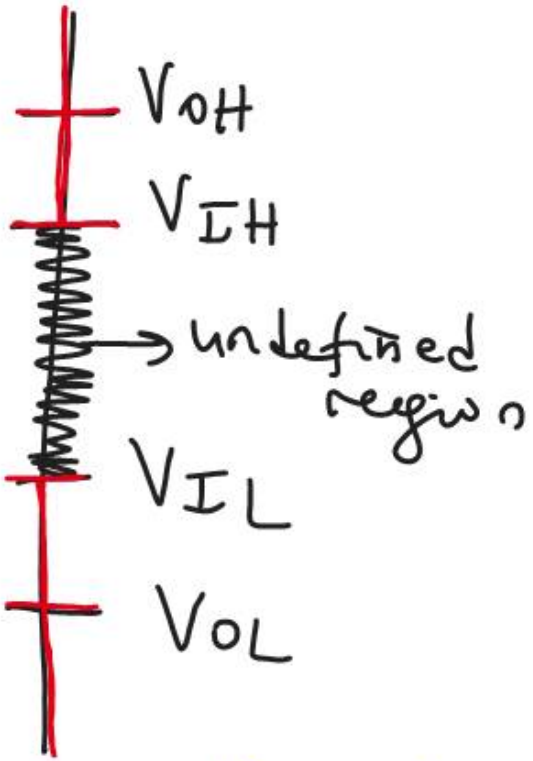
$$\text{Cost of a die} : \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}$$

$$\text{die yield} = \frac{\text{healthy dies}}{\text{Total \# of dies that can be obtained from the wafer}}$$

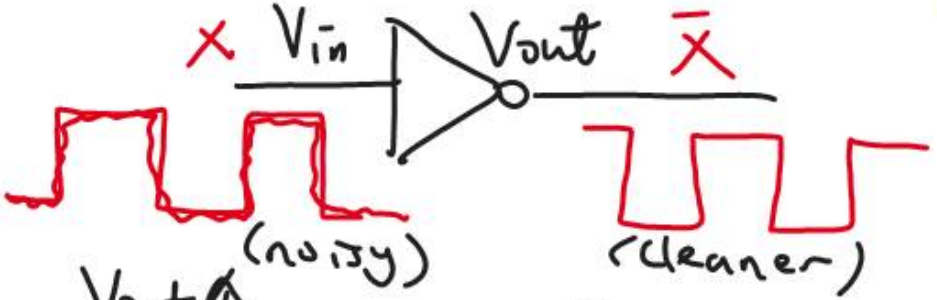
$$\text{Cost of a die} \propto f(\text{die area})^4$$

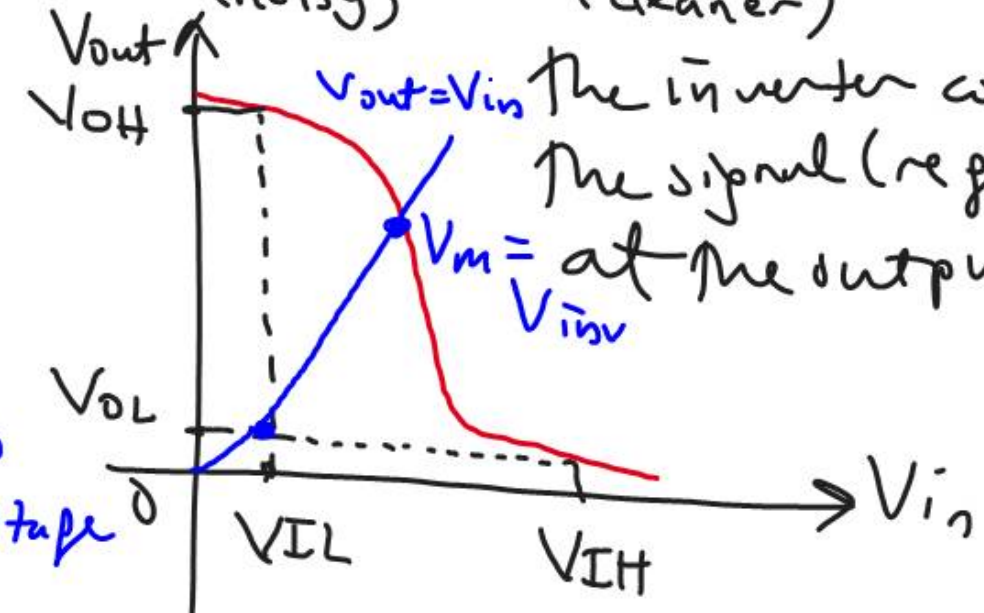
NOISE: unwanted variations of voltages and currents at the logic nodes.

NOISE MARGINS



an Inverter's Voltage-Transfer Characteristics (VTC)





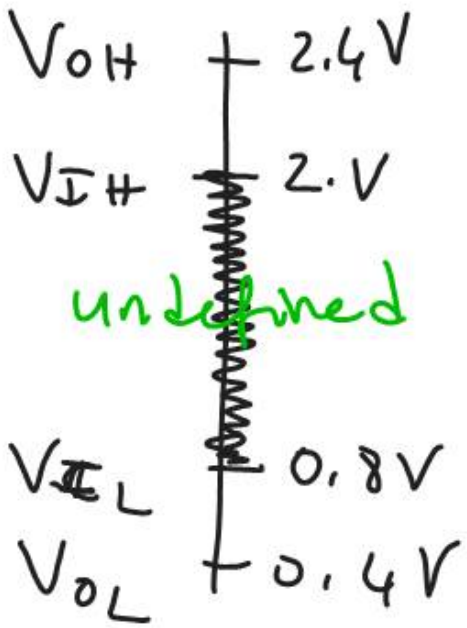
The inverter corrects the signal (regenerates)

V_M = switching threshold voltage

$$N_{mL} = V_{IL} - V_{OL}$$

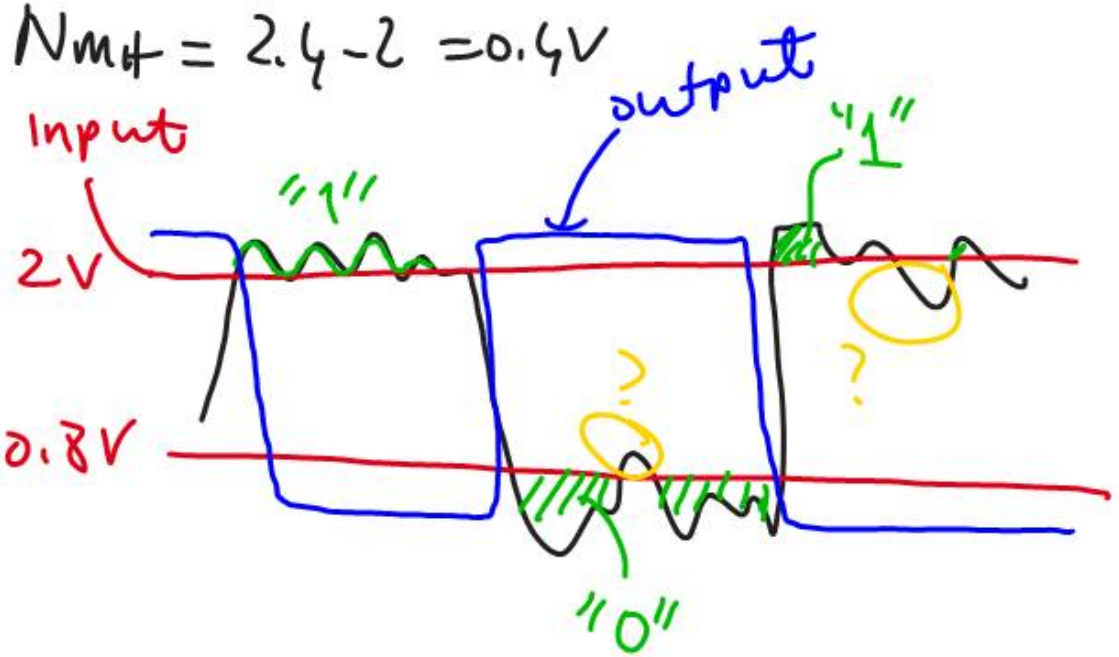
$$N_{mH} = V_{OH} - V_{IH}$$

for the TTL logic

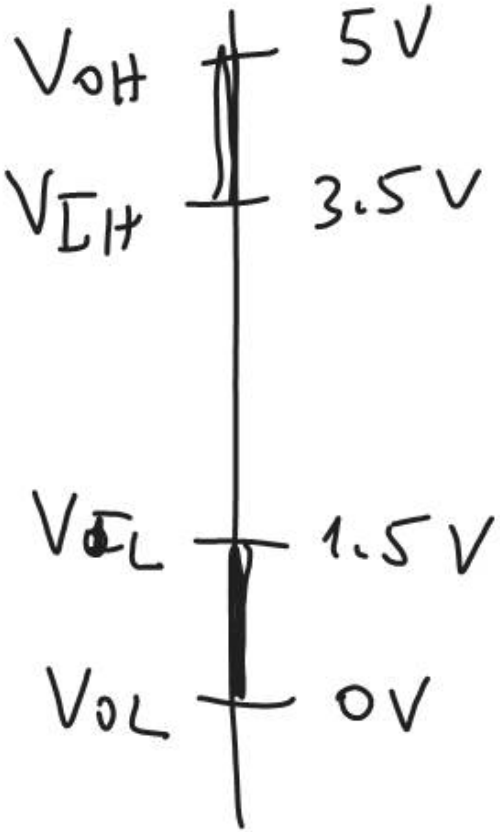


$N_{mL} = 0.8 - 0.4 = 0.4V$

$N_{mH} = 2.4 - 2 = 0.4V$



for CMOS Logic



$N_{MH} = 5 - 3.5 = 1.5V$

$N_{ML} = 1.5 - 0 = 1.5V$

as N_M ↑ then the capability of regeneration increases

The Higher the N_M the better. ✓

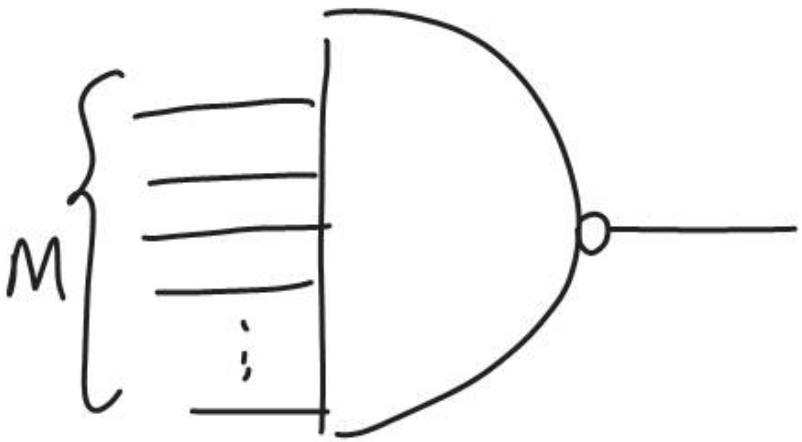
NOISE IMMUNITY: expresses the ability of the system to process and to transmit information correctly in the presence of noise.
(the rejection of noise)

Whereas Noise Margin refers to OVERPOWERING the noise

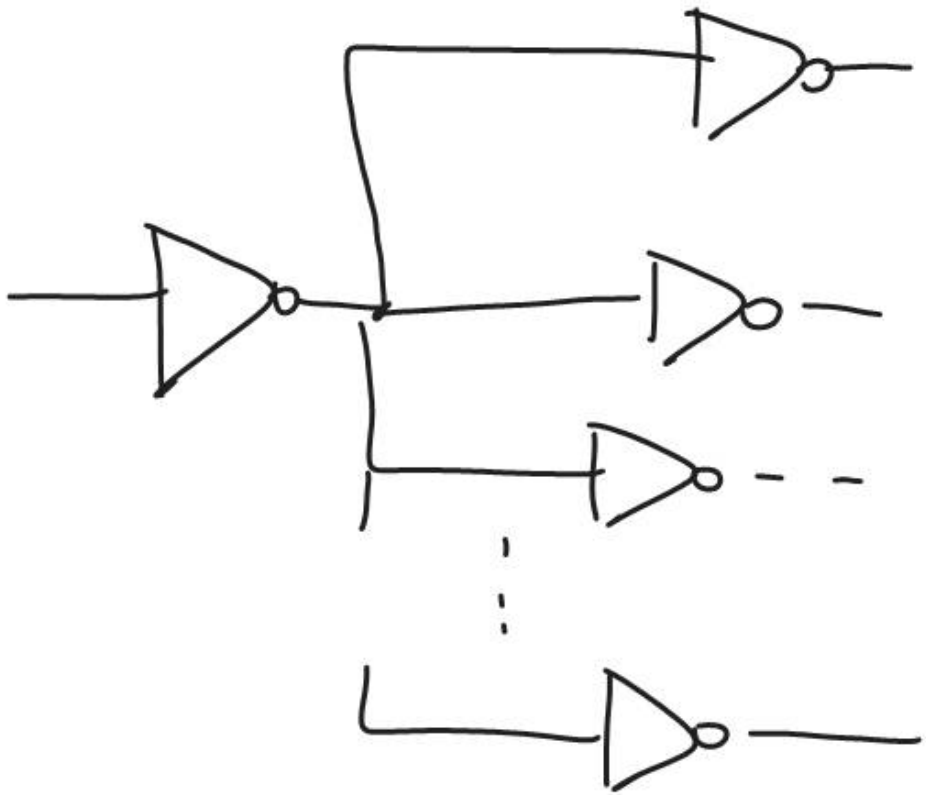
DIRECTIVITY: a gate should be UNIDIRECTIONAL.

changes in the output level should not affect or should not appear at the input.

Fan-in, Fan-out



Fan-in is M



Fan-out is n m gates

Performance

- computational ability (instructions per second)

  ~ 10 MIPS by a processor X

- CLOCK RATE (FREQUENCY)

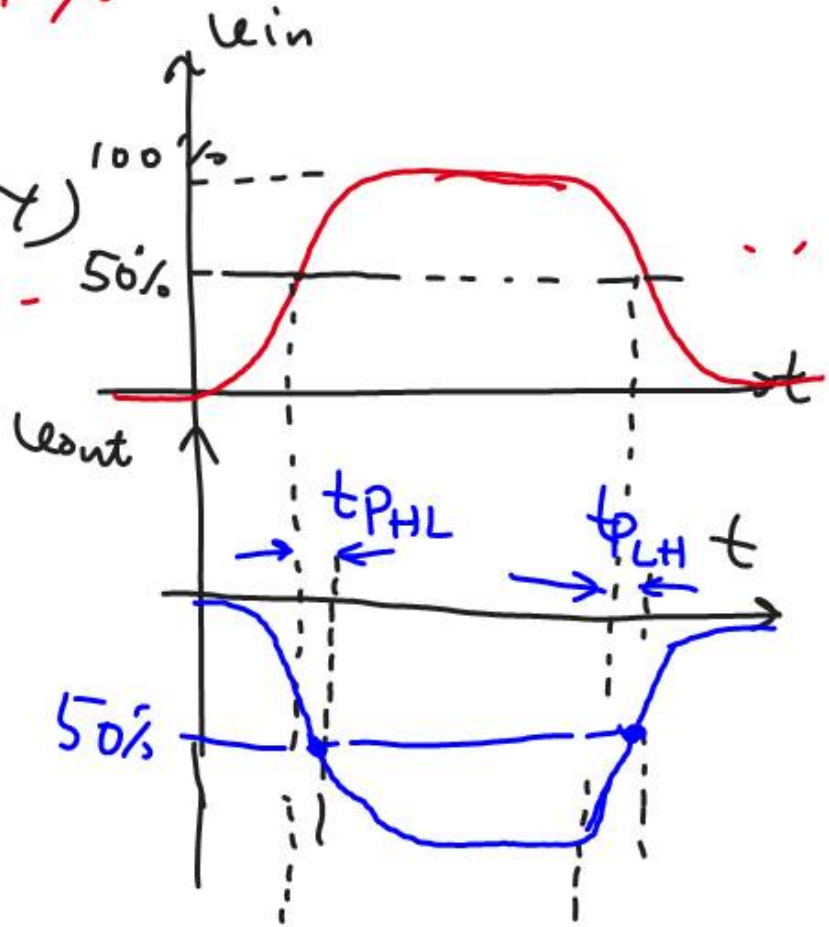
  CLOCK

propagation time t_p (delay)

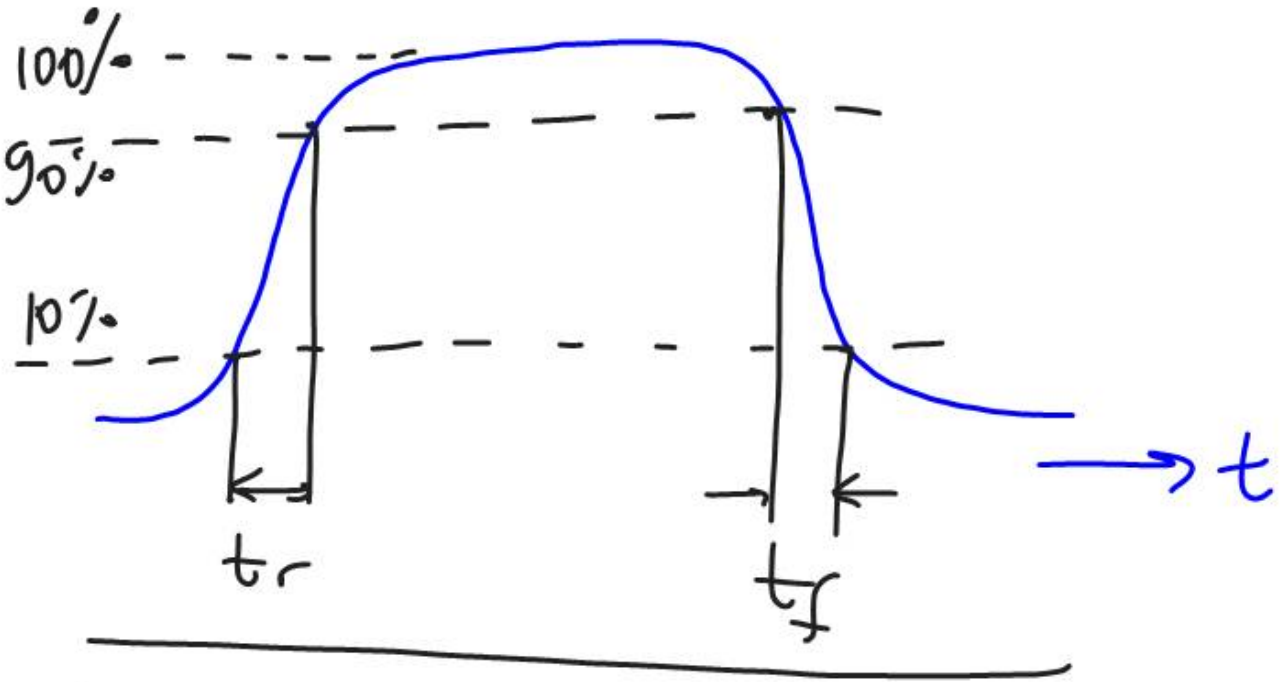
$$t_p = \frac{t_{PHL} + t_{PLH}}{2}$$

$\equiv$

t_p of a gate

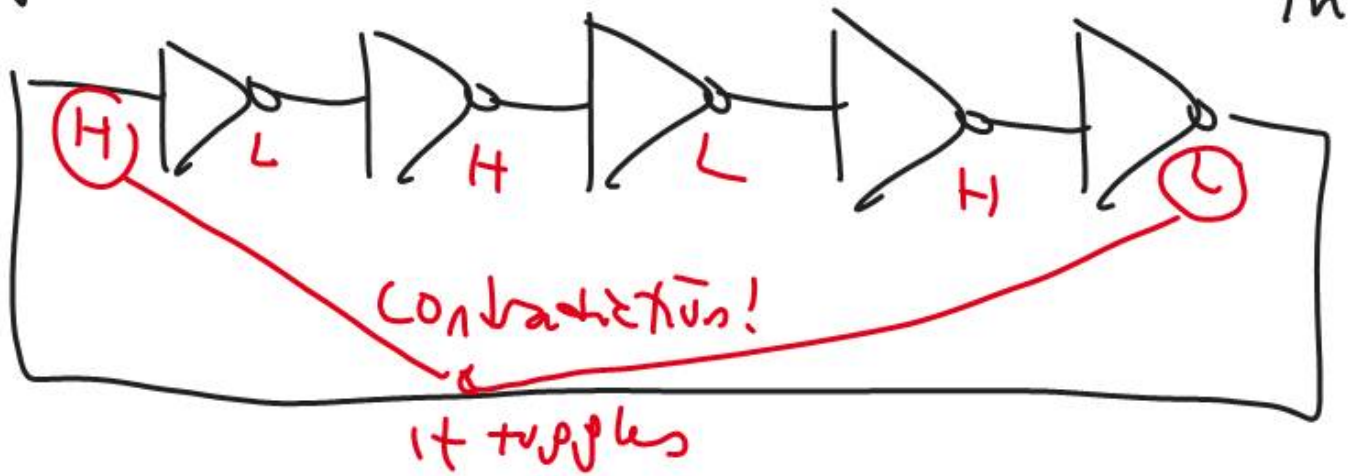


Rise time fall time of a signal



tp of a RING OSCILLATOR:

Odd number of inverters cascaded

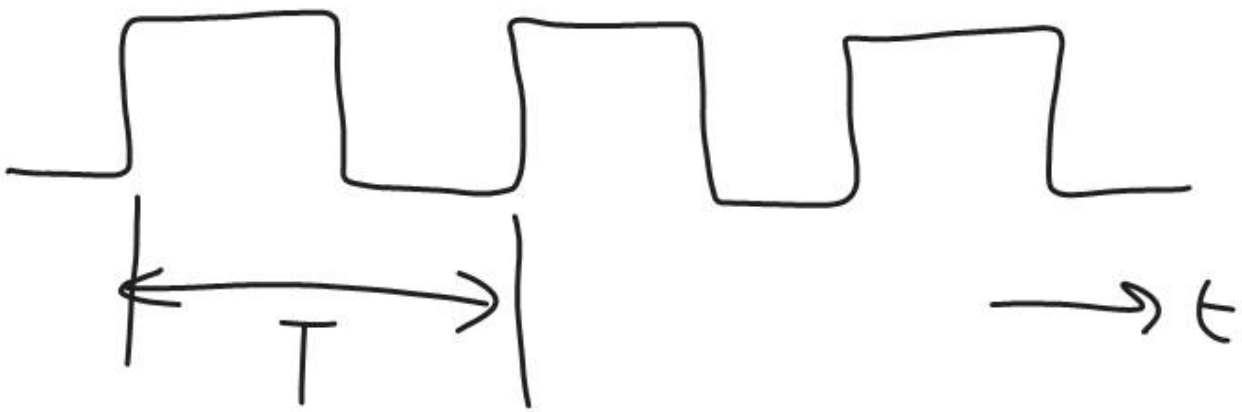


The period of the oscillation: T

$$T = 2 \times t_p \times N$$

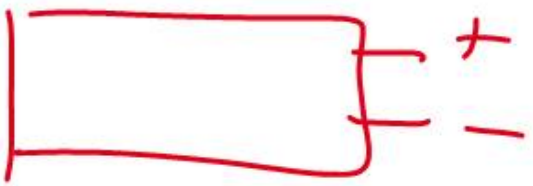
t_p = propagation time of the inverter

N = # of inverters



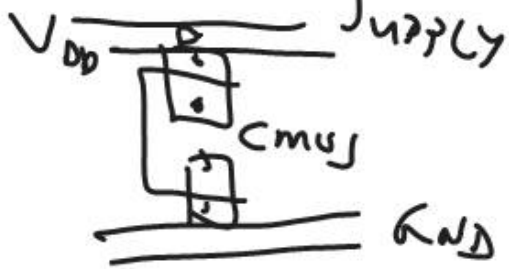
ENERGY (POWER) CONSUMPTION

- Battery for ops



10 Ah

1 A for 10 hours
or
5 A for 2 hours
or
10 A for 1 hour



- how much energy is consumed per operation
- how much heat the circuit dissipates per operation

CRITICAL DESIGN DECISIONS:

- power supply capacity
- the battery life time
- supply line sizing
- packaging & cooling requirements

POWER DISSIPATION: Is an important property of design that affects:
- feasibility
- cost
- reliability (MTBF)

DIFFERENT PROBLEMS necessitate DIFFERENT MEASURES

Supply line sizing → Peak Power P_{peak}

Cooling or battery requirements → Average power consumption P_{ave}

$$P_{peak} = i_{peak} \cdot V_{supply} = \max P(t)$$

$$P_{ave} = \frac{1}{T}\int_0^T P(t)\,dt = \left(V_{supply}/T\right) \cdot \int_0^T i_{supply}(t)\,dt$$

Power Dissipation

- Static (all the time)
- Dynamic (during switching)

$P(t) = v(t) \cdot i(t)$

$= V_{supply} \cdot i(t)$

* → very important to reduce this!

$i(t) = \frac{dq}{dt} = q \cdot \frac{dn}{dt}$

$1.6 \times 10^{-19} C$ for an e^-

* The PROPAGATION DELAY and the POWER CONSUMPTION are RELATED!

t_p: time at which given amount of energy can be stored in the gate capacitances.

$q = C \cdot v$ $\quad i = \frac{dq}{dt} = C \cdot \frac{dv}{dt}$

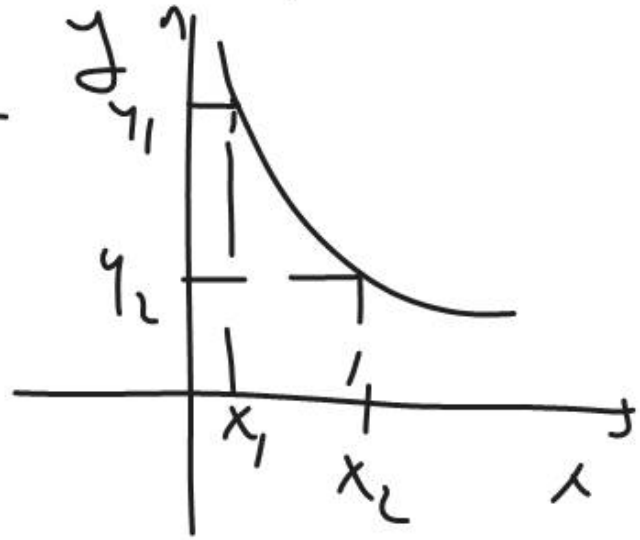
Propagation Delay X Power Consumption = CONSTANT

Power Delay Product (PDP) ⇒ Very important measure!

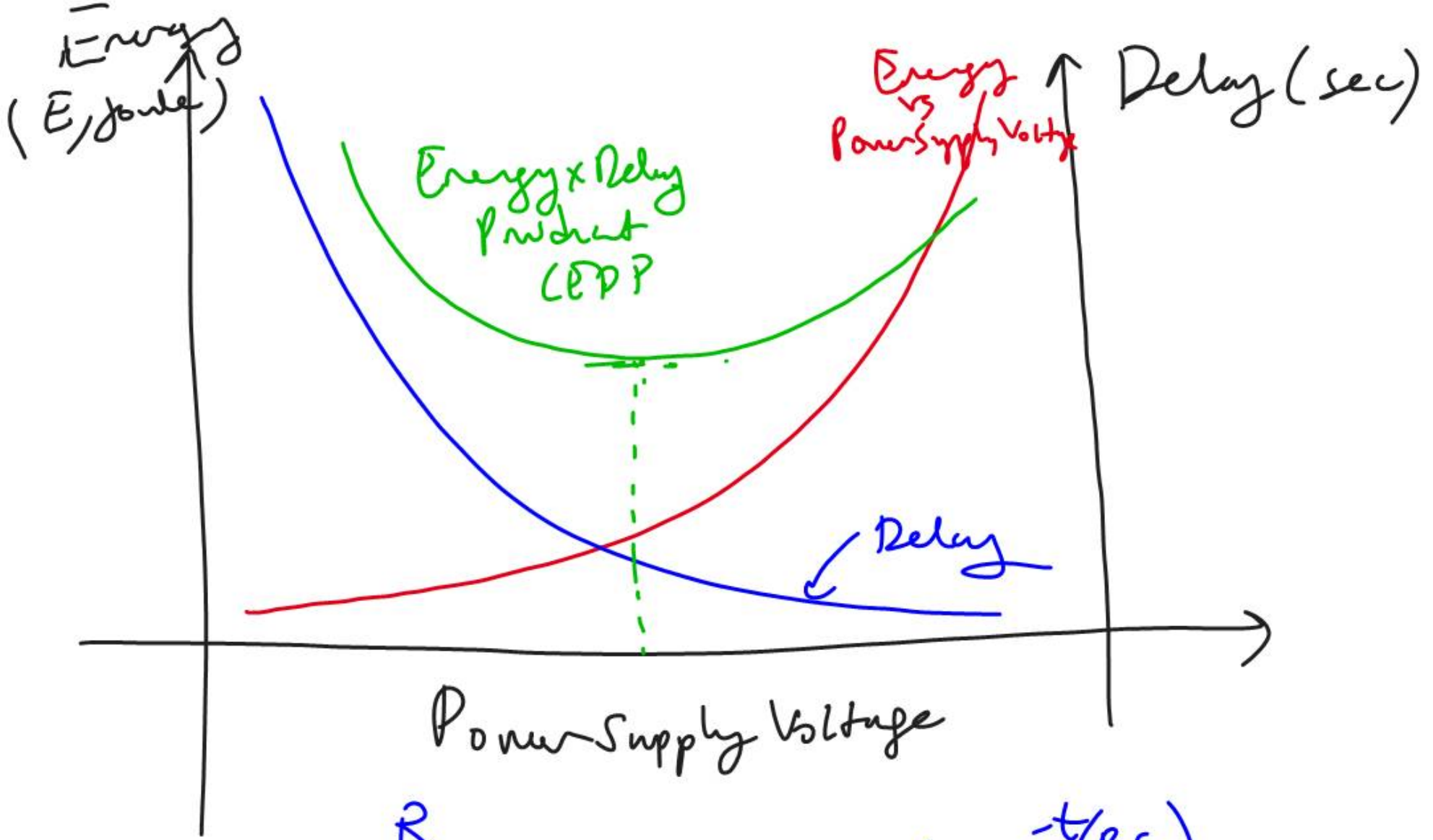
Energy Delay Product (EDP)

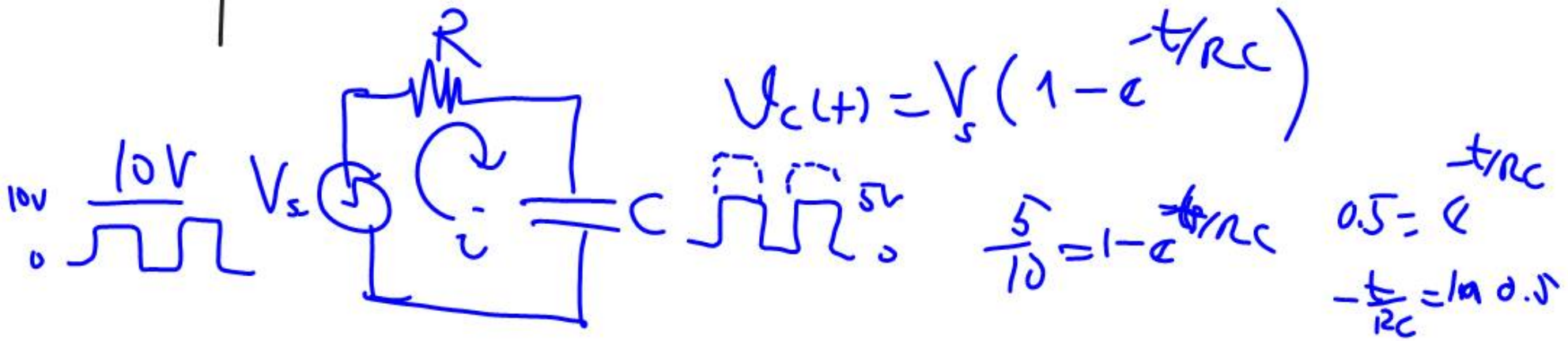
Ultimate Quality Metric

$x \cdot y = \text{const}$



EDP / PDP



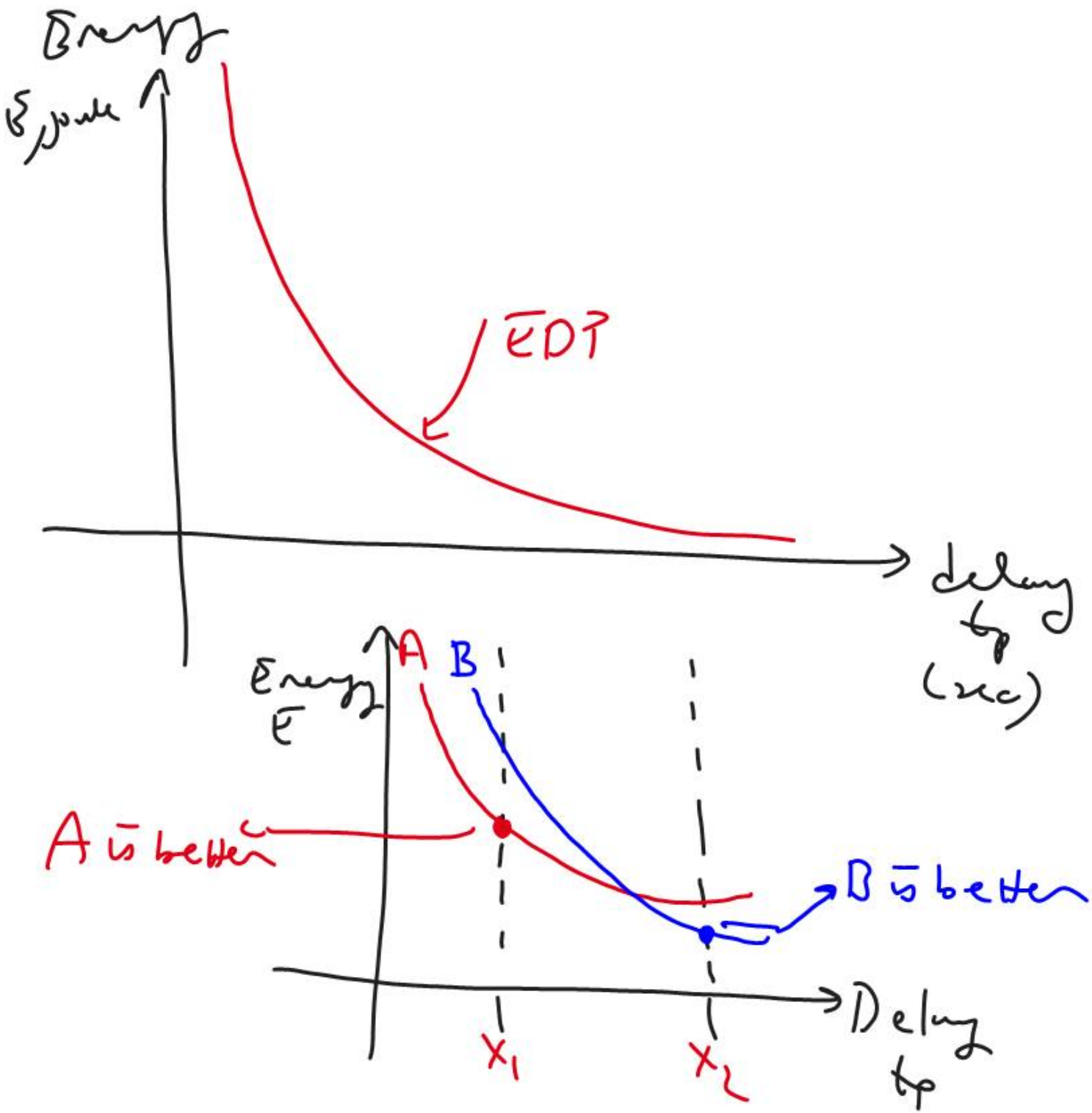


$$V_c(t) = V_s\left(1 - e^{-t/RC}\right)$$

$$\frac{5}{10} = 1 - e^{-t/RC}$$

$$0.5 = e^{-t/RC}$$

$$-\frac{t}{RC} = \ln 0.5$$


Energy
EDT
delay
tp
(sec)
Energy
E
A
B
A is better
B is better
X1
X2
Delay
tp