05.11.2019

$R_d = g\, R_{ch}$

We have to reduce the channel resistance of the pull-down transistor!

OR we have to increase the conductance of the pull-down transistor.

$$I_d = \beta\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \qquad \text{in linear (LIN) region}$$

$$I_d = \frac{\beta}{2}\left(V_{GS} - V_T\right)^2 \qquad \text{in SAT. region}$$

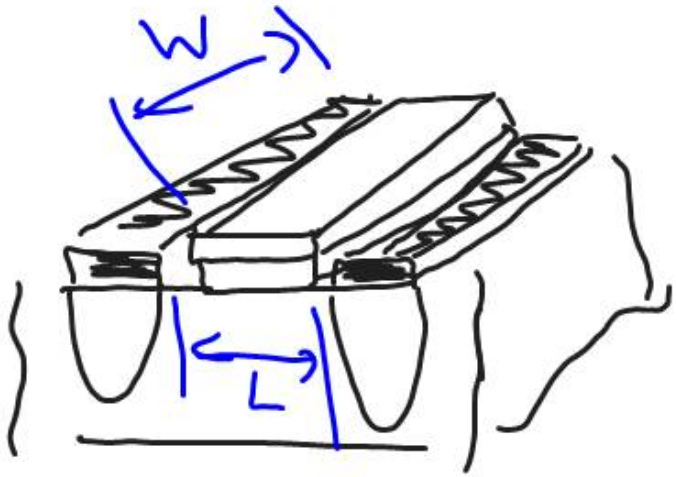
$$G = \left.\frac{\partial I_d}{\partial V_{DS}}\right|_{V_{GS}=\text{const}} \longrightarrow \alpha\,\beta$$

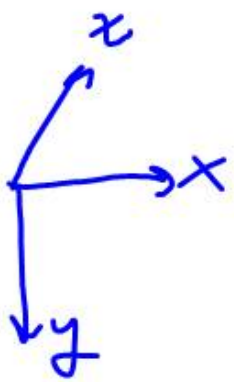
$$\beta = \frac{\epsilon \cdot \mu}{t_{ox}} \left(\frac{W}{L} \right) \Longrightarrow$$ Channel width W will be increased to improve the conductance of the channel (transistor)

Increasing W $\Longrightarrow$ bigger transistor!

(consumes die area)

↳ expensive!



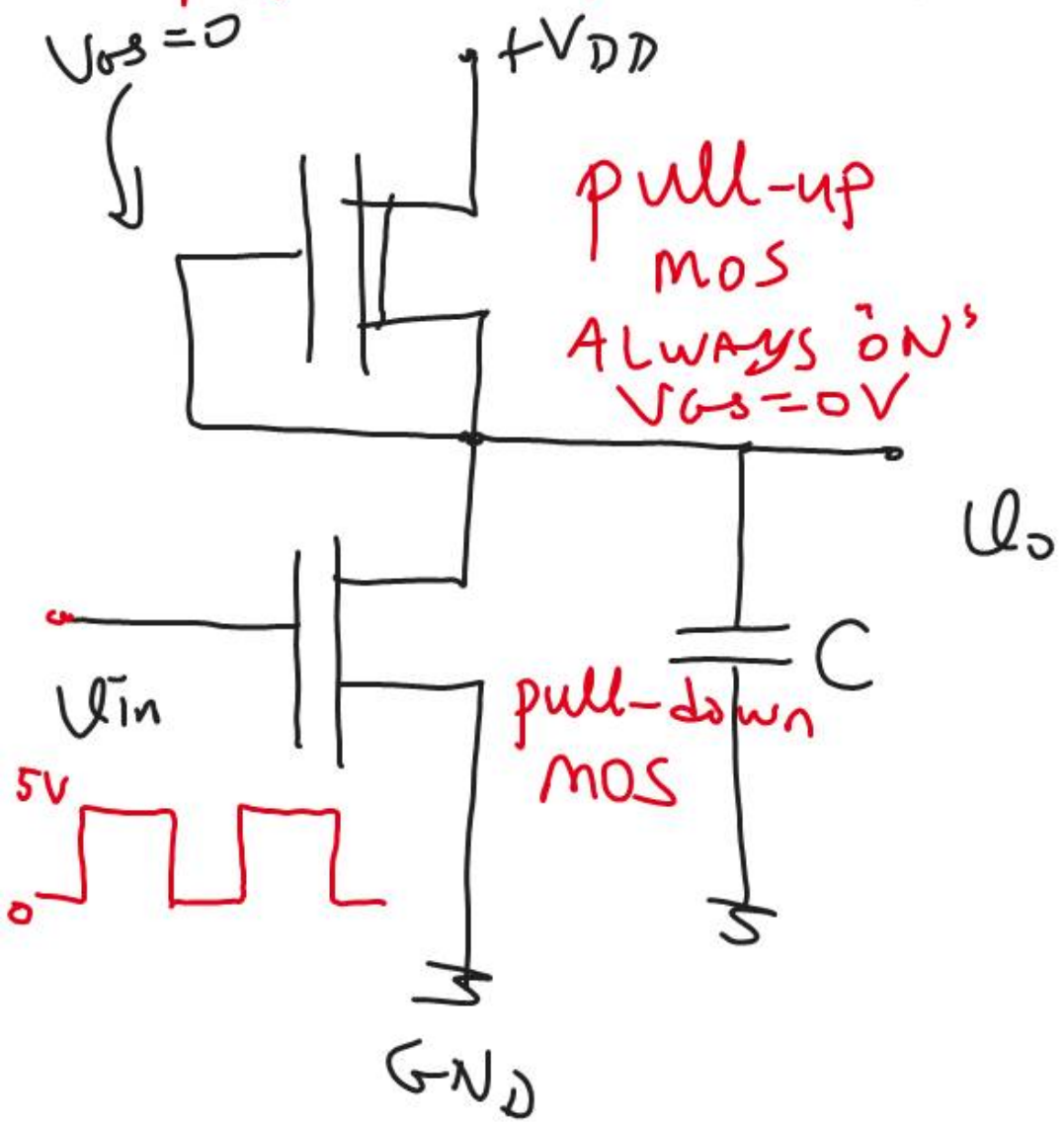


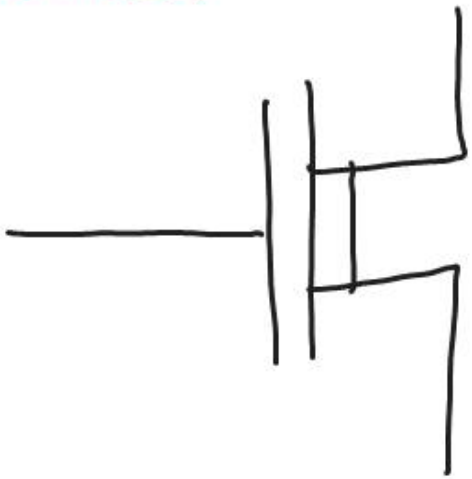
Therefore (:-) ⇒ Basic inverter is not good!

- Static electricity consumption is HIGH (Energy consumption is very HIGH)
- transients are not symmetric
- to decrease V_{DSL}, W should be increased the transistor gets BIGGER and BIGGER which is not good!

We have to be SMARTER

② Inverter with an Depletion-mode n-channel MOS as pull-up device:





n-channel DEPLETION mode MOSFET

This transistor is ON at $V_{GS}=0V$.

$(V_T = -V_{dep})$

< 0

Problem: When the pulldown NOS becomes ON since the pull-up MOS is always "ON", a path from V_{DD} to GND is formed again. → Static current will flow ⇒ Energy is consumed again!

So we couldn't get rid of this problem with this circuit as well.

It persists!

However, it brings some advantages though.

Depletion mode n MOS

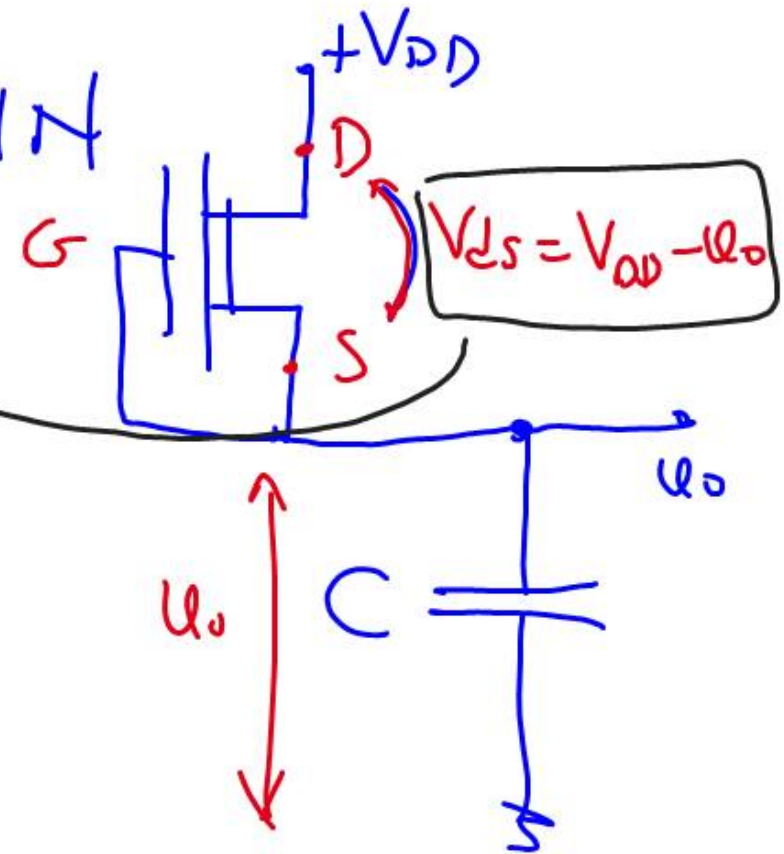
$$V_{GS} - V_T = V_{GS} - (-V_{dep})$$

$$= 0 + V_{dep}$$

$$V_{GS} - V_T = V_{dep}$$

$$I_d = \frac{\beta_{pu}}{2} |V_{dep}|^2 \quad \text{SAT}$$

$$I_d = \beta_{pu} \left(V_{dep} - \frac{V_{ds}}{2} \right) V_{ds} \quad \text{LIN}$$

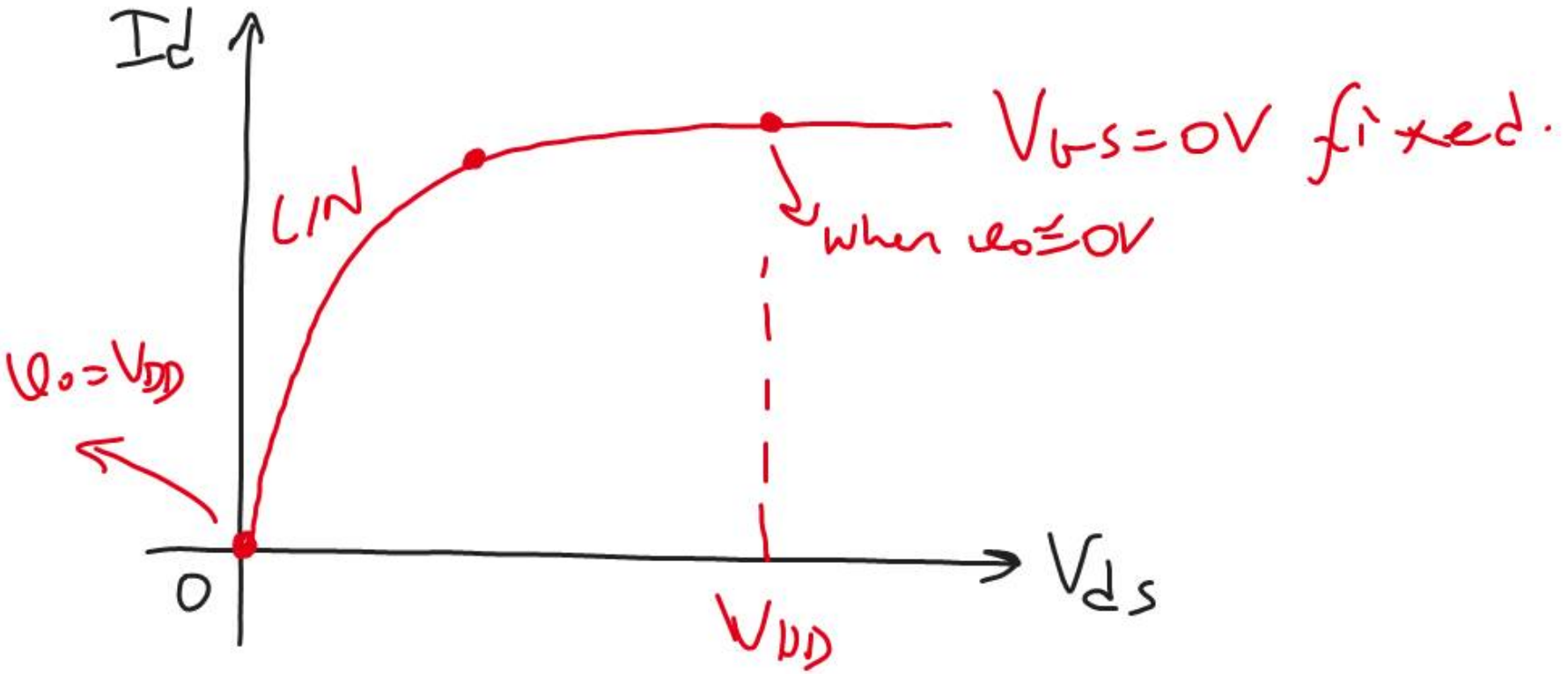


Before discharge we have

$V_o = V_{DD} \longrightarrow V_{ds} = V_{DD} - V_{DD} = 0$

When capacitor discharges to V_{oL}

$V_o = V_{oL} \approx 0V \longrightarrow V_{ds} \cong V_{DD}$



when $v_o = V_{DD} \rightarrow V_{DS} = V_{DD} - V_{DD} = 0$ $I_d \rightarrow 0$

when $v_o \cong v_{oL} \cong 0 \rightarrow V_{DS} \cong V_{DD} - 0 \cong V_{DD}$ $I_d \rightarrow$ big

SATURATION

For the pull-down MOS

$I_d = 0$ when $V_{GS} - V_T \leq 0$ CUT-OFF

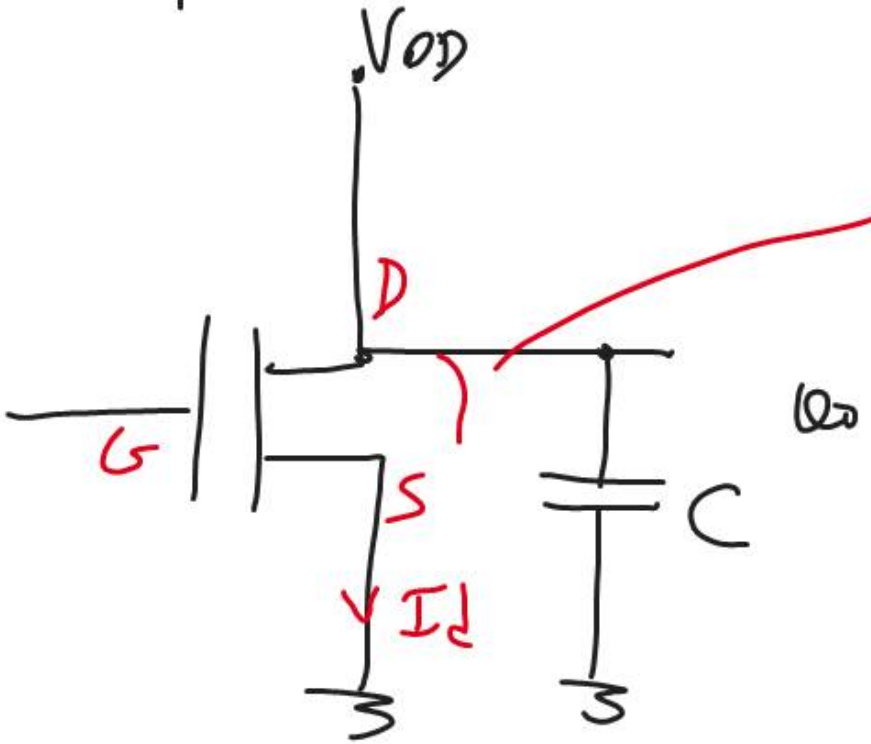
$$I_d = \beta_{pd}\left(V_{GS} - V_T - \frac{V_{ds}}{2}\right) \cdot V_{ds}$$ when $V_{GS} - V_T \geq V_{ds}$

LINEAR (LIN)

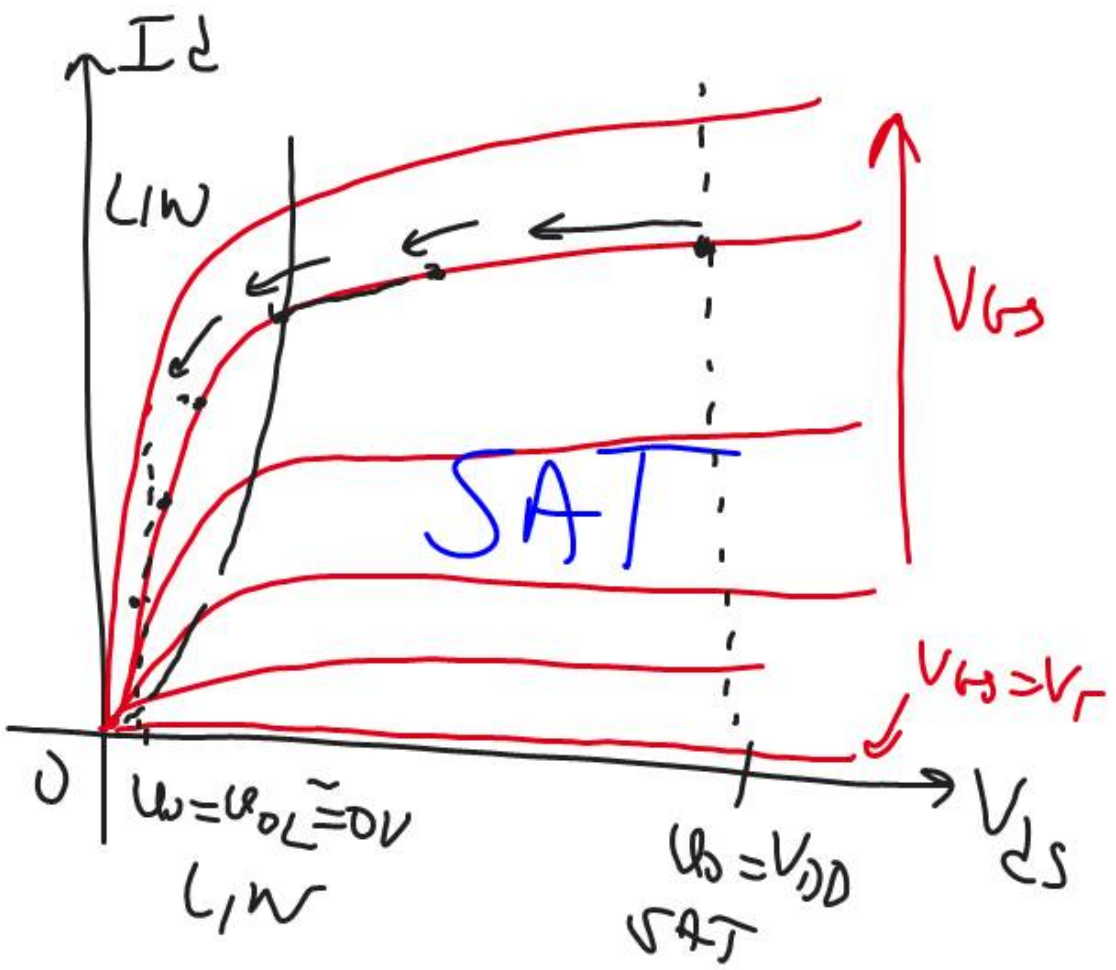
$$I_d = \frac{\beta_{pd}}{2}(V_{GS} - V_T)^2$$ when $V_{GS} - V_T < V_{ds}$

SATURATION (SAT)

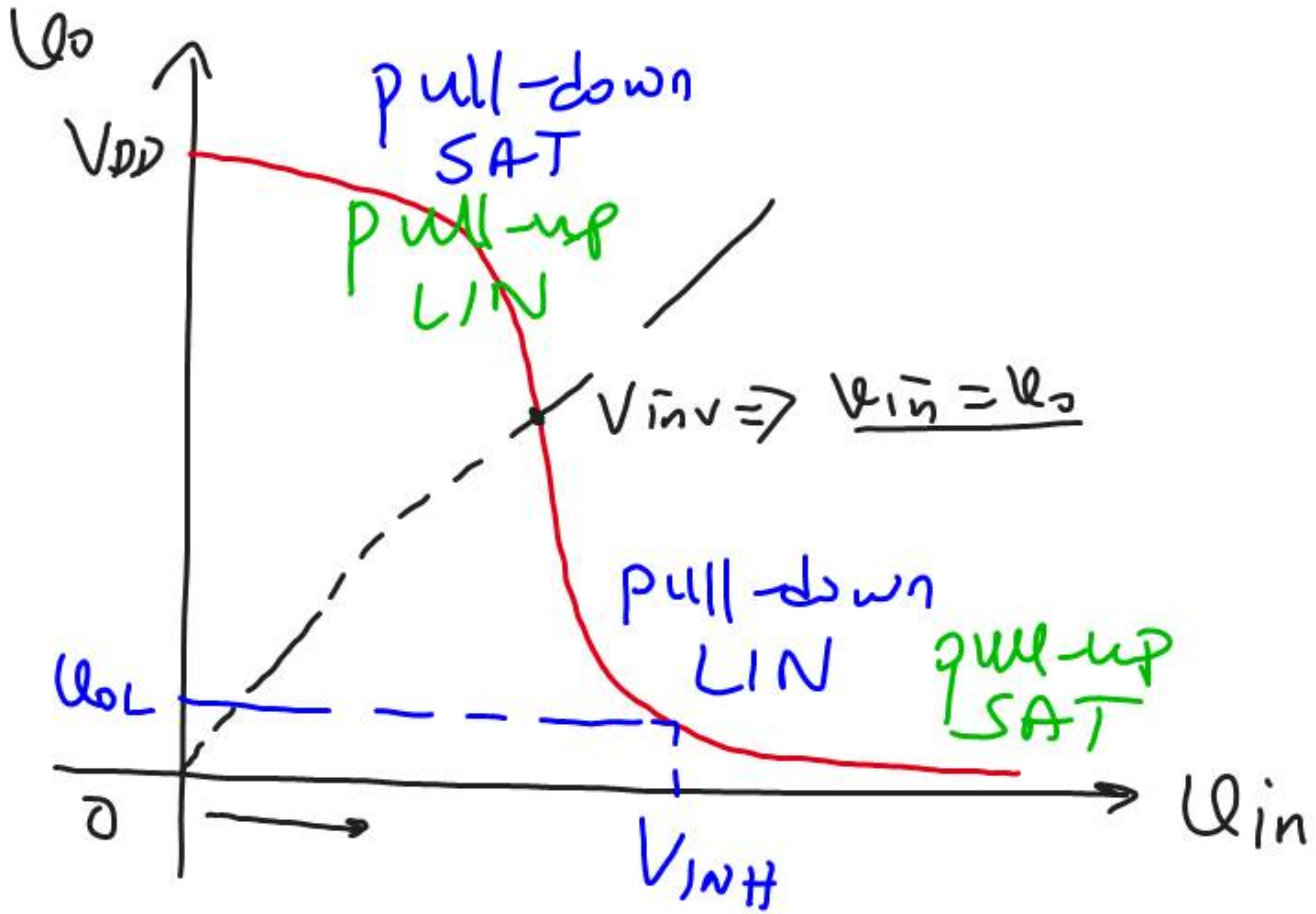
PULL-DOWN nos



$V_o = V_{ds}$ of the pull-down nos



VTC Voltage Transfer Characteristics of the INVERTER



When $V_o = V_{OL} \Longrightarrow$ Pull-down, pull-up is
LIN, SAT

LIN SAT

$$\beta_{pd}\left(V_{GS}-V_T-\frac{V_{ds}}{2}\right)V_{ds}=\frac{\beta_{pu}}{2}\left(|V_{dsp}|\right)^2$$

When $v_o=v_{oL}$ $\rightarrow$ $V_{in}=V_{DD}$

$V_{ds}=v_{oL}$ (for pull-down) $\Rightarrow$ $V_{GS}=V_{DD}$

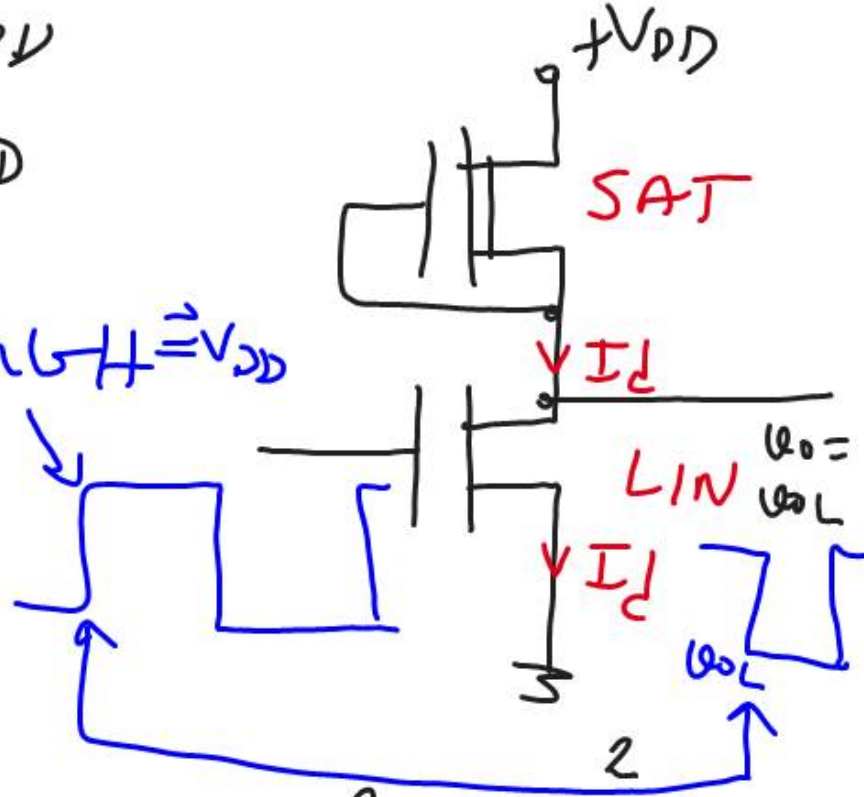
$$\beta_{pd}\left(V_{DD}-V_T-\frac{v_{oL}}{2}\right)v_{oL}$$

$$=\beta_{pu}\left(V_{dsp}\right)^2$$

$V_{DD}\gg V_T$ $\rightarrow$ neglect V_T

v_{oL} is low $\rightarrow$ neglect $\frac{v_{oL}}{2}$

$$\beta_{pd}\left(V_{DD}\right).v_{oL}\cong\frac{\beta_{pu}}{2}\left(V_{dsp}\right)^2$$

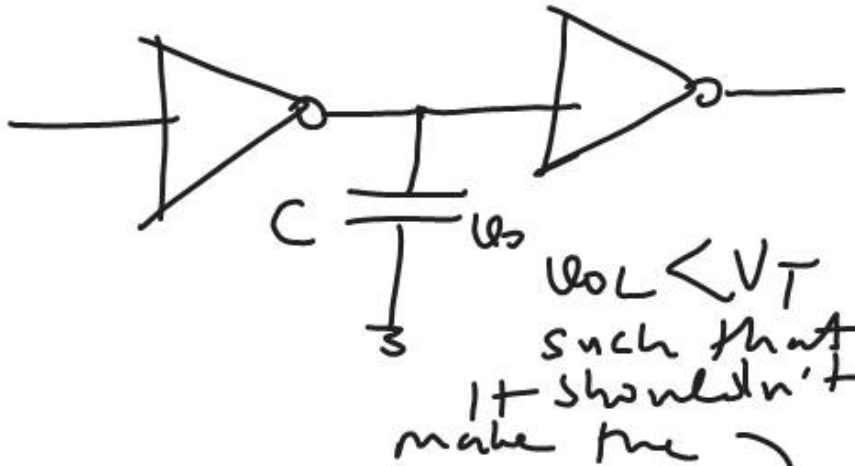


$$v_{oL}\cong\frac{\beta_{pu}}{2\beta_{pd}}\frac{2\,V_{dsp}}{V_{DD}}$$

$$V_{OL} \cong \frac{\beta_{pu} \cdot V_{dsp}^2}{2\beta_{pd} V_{DD}}$$

or

$$V_{OL} = \frac{\beta_{pu} V_{dsp}^2}{2\beta_{pd}(V_{DD} - V_T)}$$



To make V_{OL} low enough (to reduce V_{OL})

we should either: (or both)

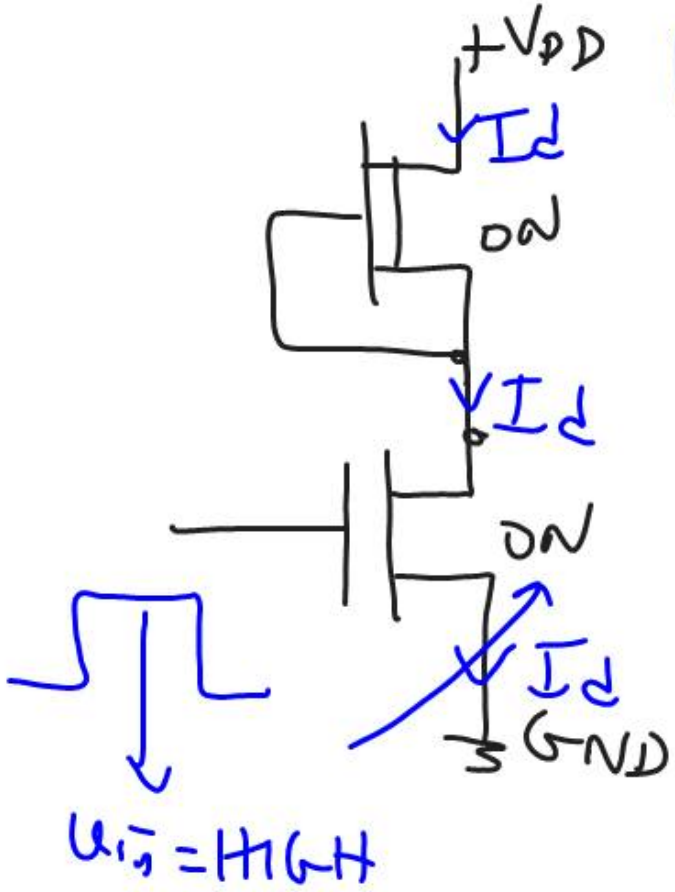
$$k = \frac{\beta_{pd}}{\beta_{pu}}$$ (Inverter Ratio)

we should increase V_{DD} (Which is not good!) $\left(E = \frac{1}{2} C V_{DD}^2\right)$

$$V_{OL} = \frac{1}{2k} \frac{(V_{dd})^2}{(V_{DD} - V_T)}$$

$$k = \frac{\beta_{pd}}{\beta_{pu}} \Longrightarrow$$ increasing k means increasing the channel width of the pull-down transistor (W_{pd}) to make it BIGGER (AREA!)

Also, during the pull down transistor's ON period we have a static current flowing and a DC power consumption:



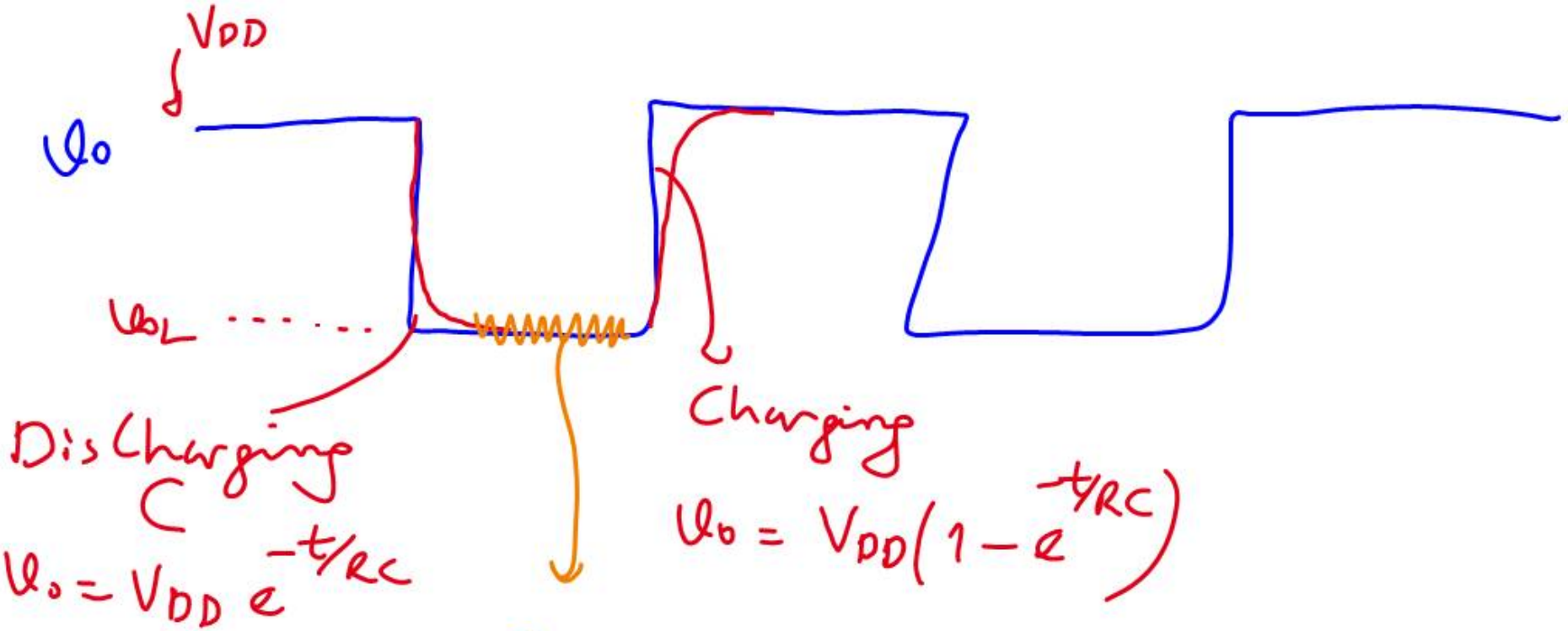
$$V_p = I_d \times V_{DD}$$

DC power loss

Static power dissipation

$$V_p = \frac{V_{DD}^2}{(R_{dpu} + R_{dpd})}$$

Effective channel resistances.

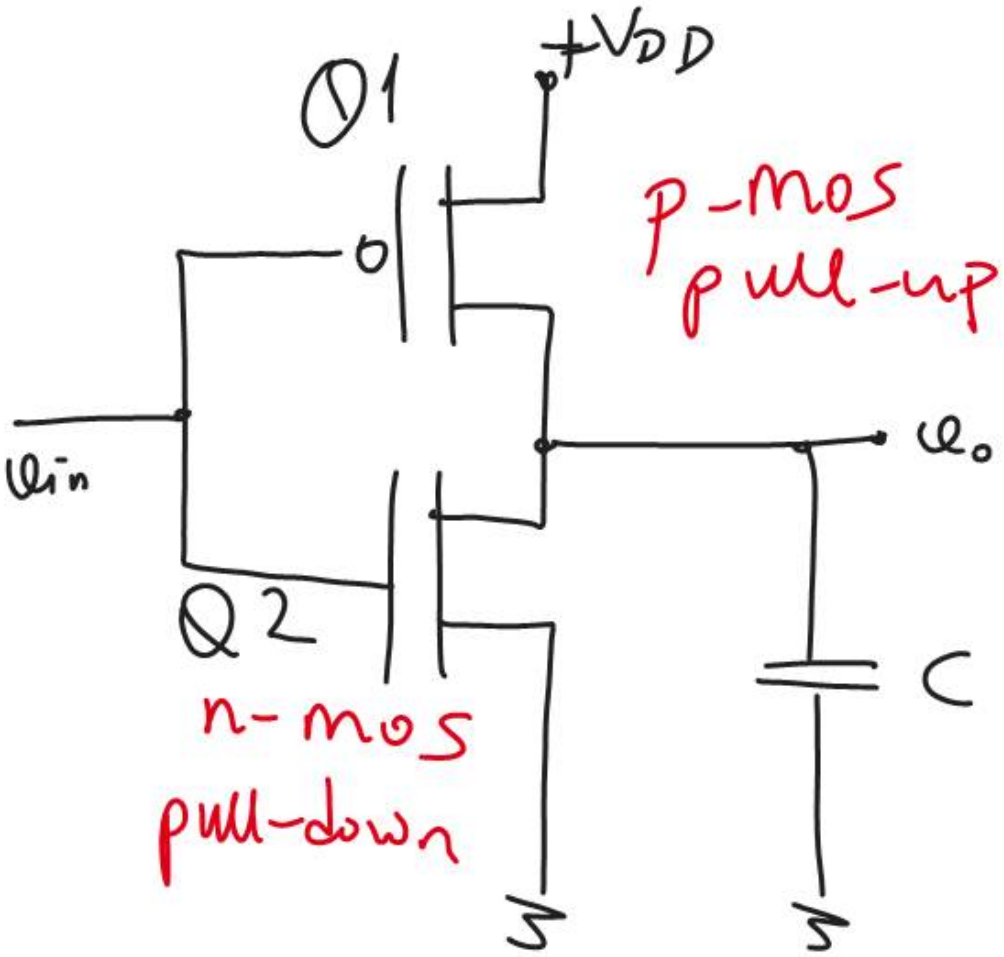


*We have a better Inverter than the basic inverter.

But, we have static power (DC power) loss again!

*and to keep VoL small, we have to make Pull-down MOS BIGGER!

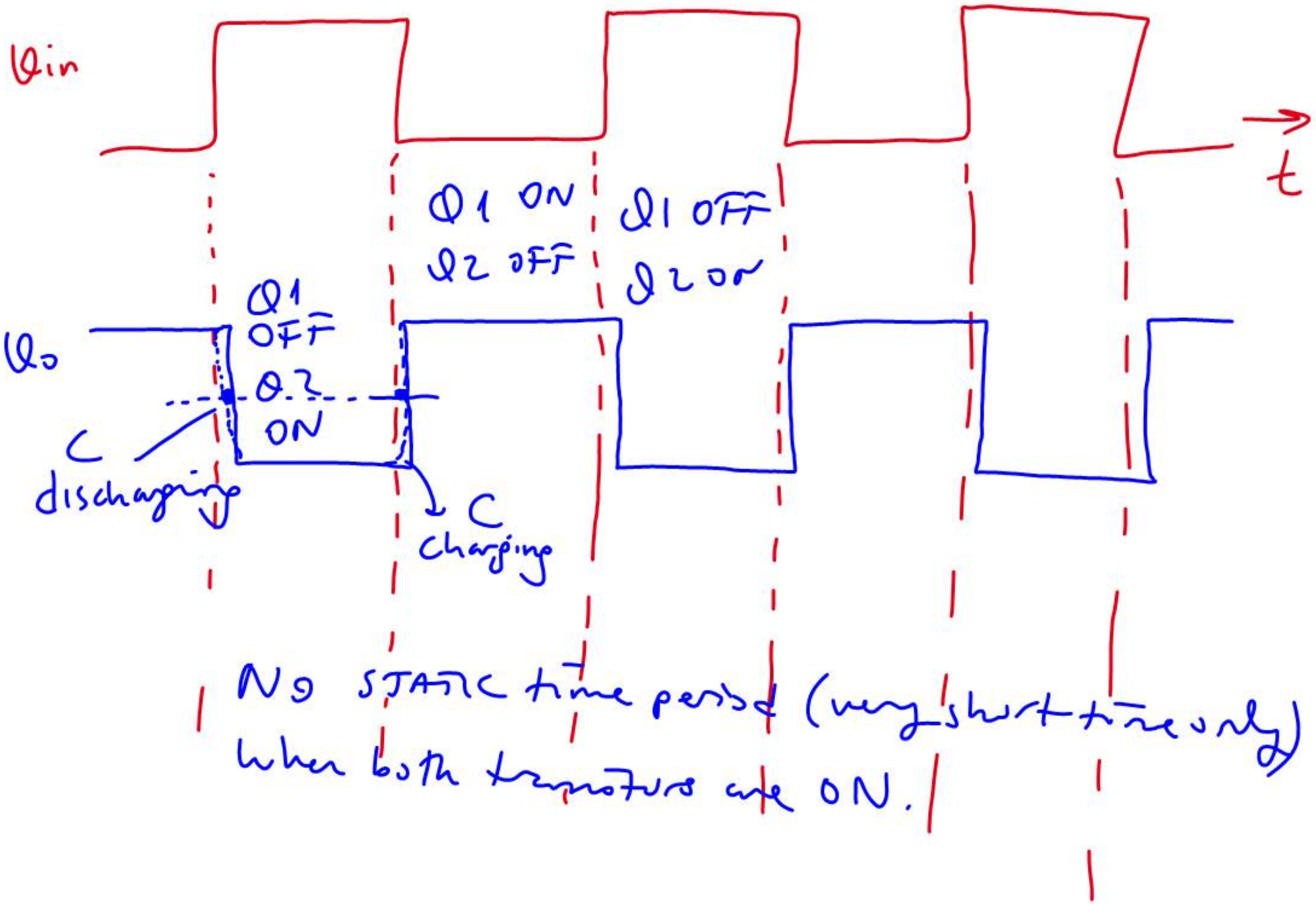
★ Better Application ⟹ CMOS INVERTER



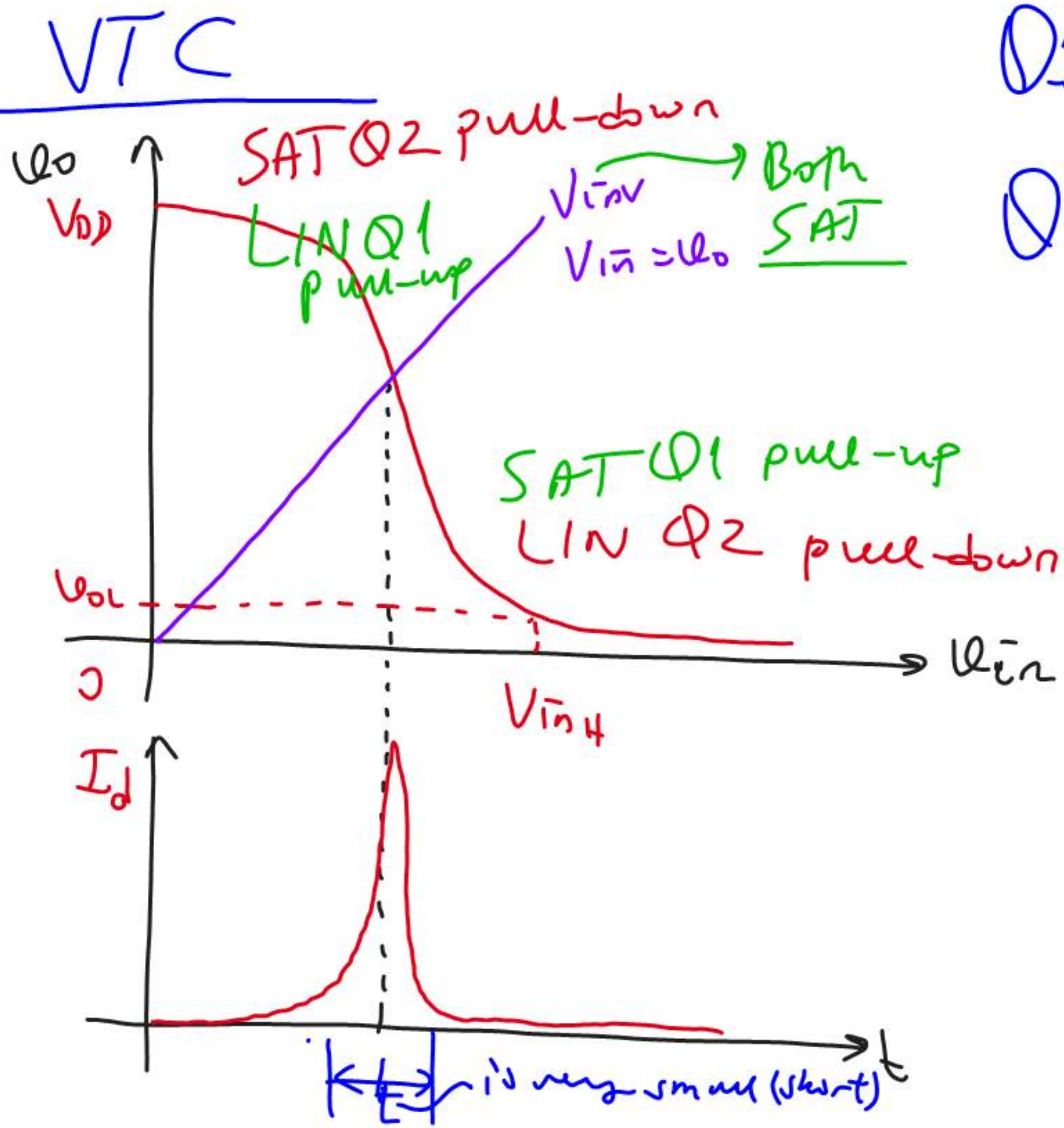
When Q1 is ON
Q2 is OFF
when Q1 is OFF
Q2 is ON

Both of them are ON in a very short instance (only during switching)

No STATIC, or DC power consumption.


V_{in}
t
Q1 ON
Q2 OFF
Q1 OFF
Q2 ON
V_o
Q1 OFF
Q2 ON
C discharging
C charging
No STATIC time period (very short time only) when both transistors are ON.

VTC

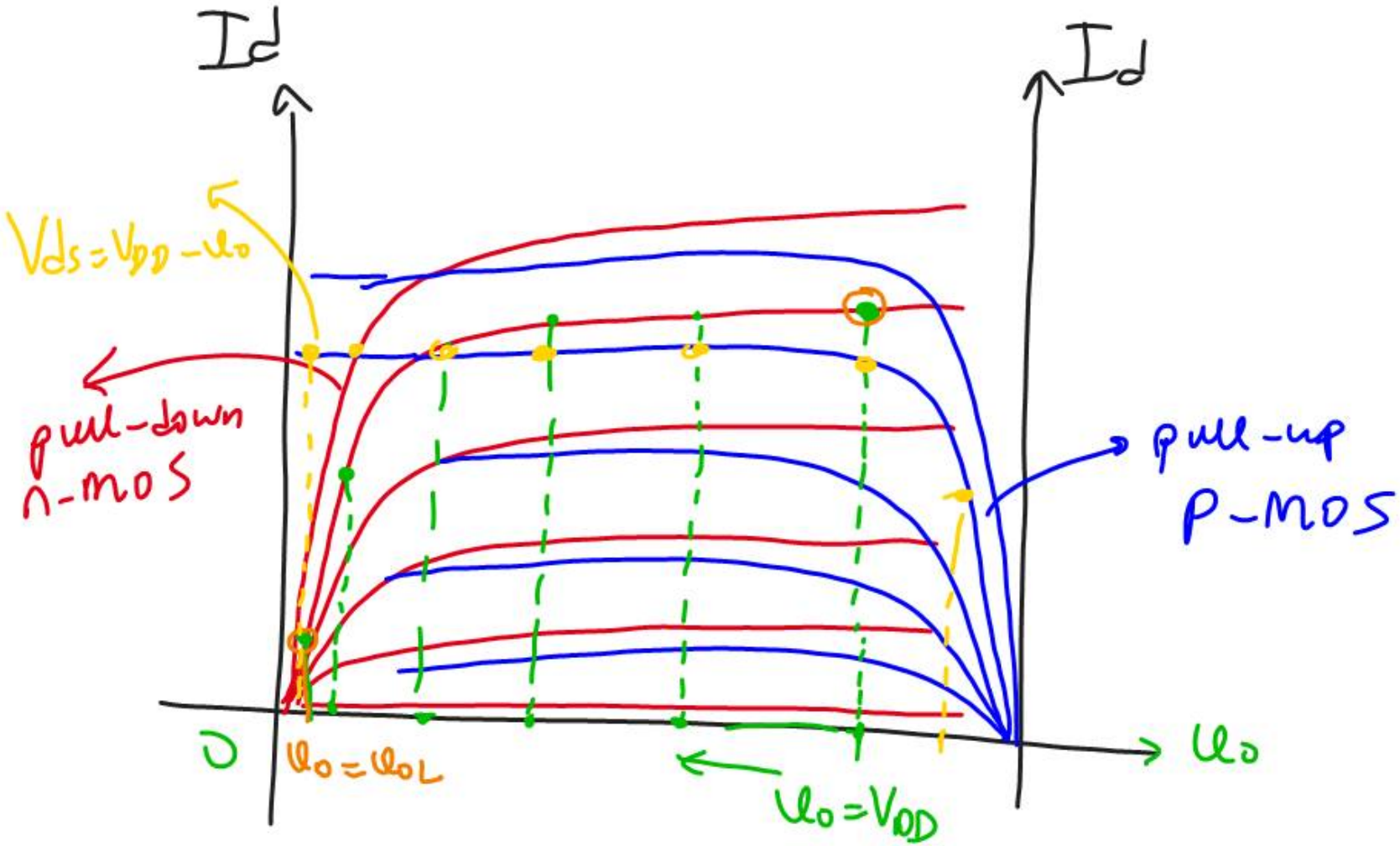


Q1 pull-up

$V_{ds} = V_{DD} - V_o$

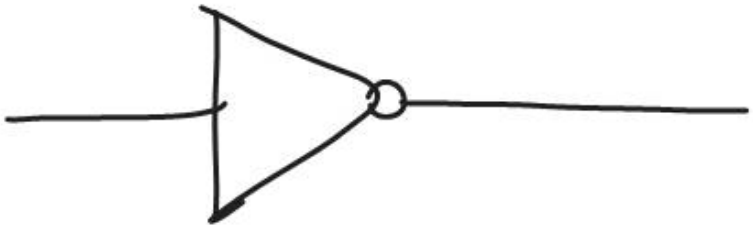
Q2 pull-down

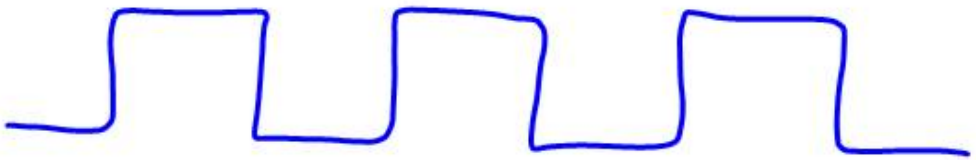
$V_{ds} = V_o$



CMOS inverter consumes power only during switching. If the clock frequency increases power consumption increases in CMOS.

example: a CMOS inverter





$\phi_1 \Rightarrow f = 1\,GHz$

$\phi_2 \Rightarrow f = 4\,GHz$

CMOS inverter consumes 4 times bigger Power at this frequency than it does at 1 GHz.

However in this case (CMOS inverter), to a certain extent, we have no pressure on the design of the pull-down transistor. (to keep V_{OL} lower)

problem: p-mos transistor has lower hole transitor (holes are slower than electrons) (speed)

this causes smaller I_d, other factors kept constant, in p-MOS. We have to make p-MOS a little bit larger than n-MOS to balance this. (1.5/1)