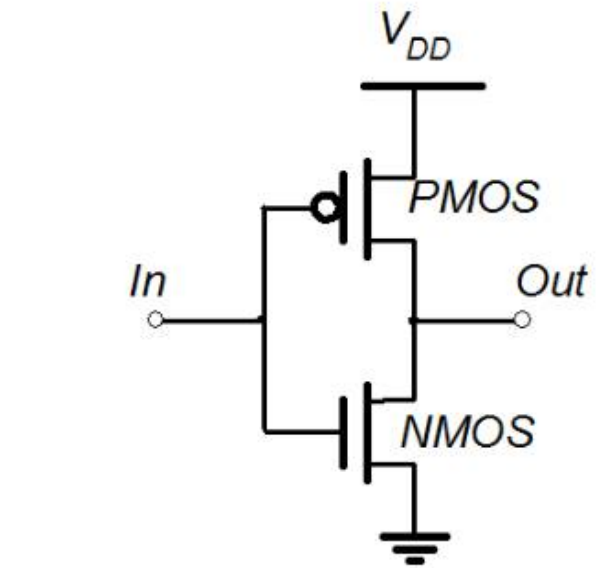
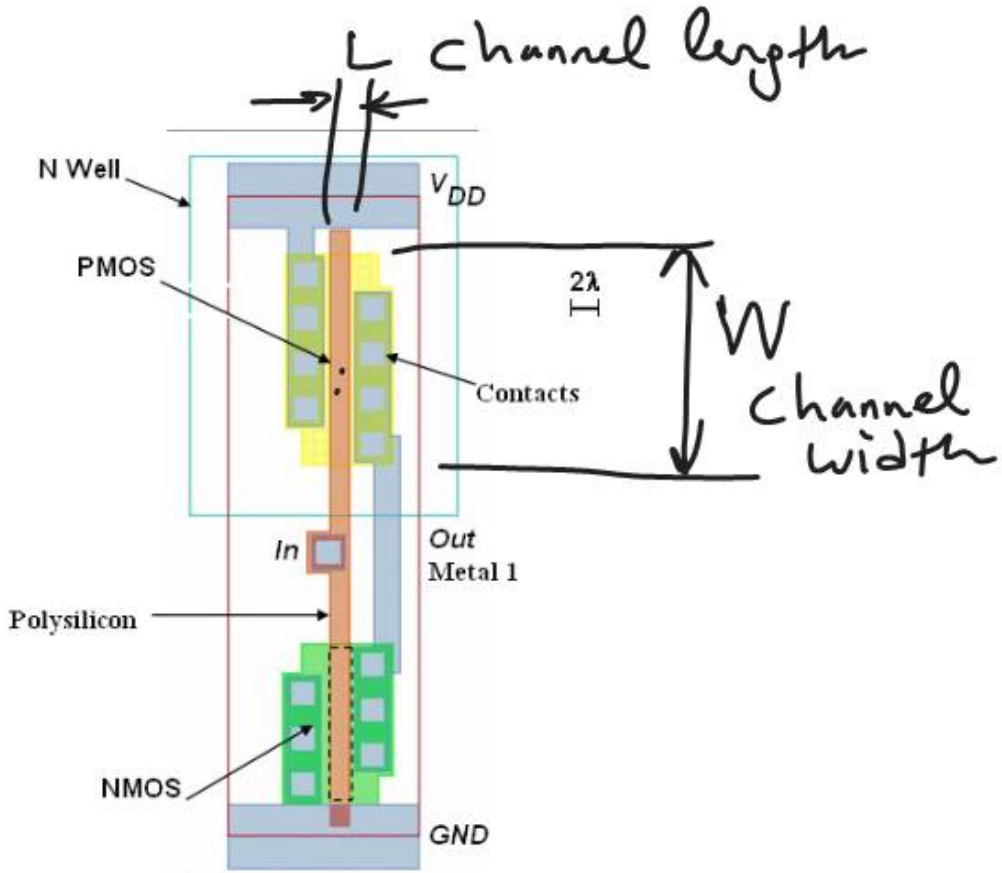
12 Nov 2010

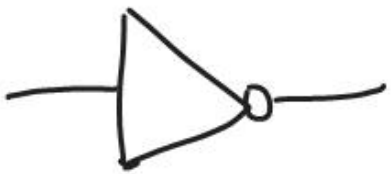
A CMOS INVERTER

(c)

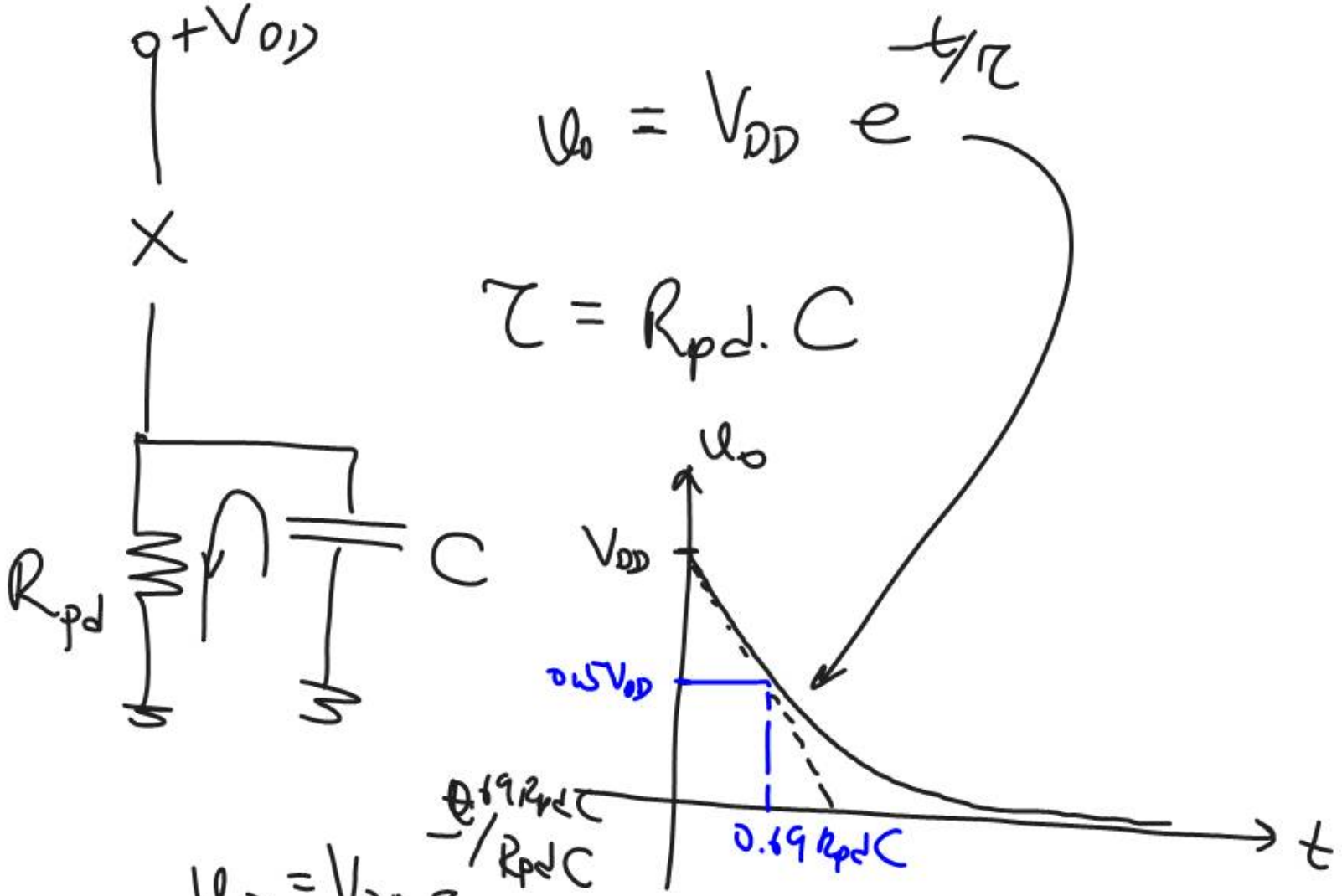
CMOS Inverter

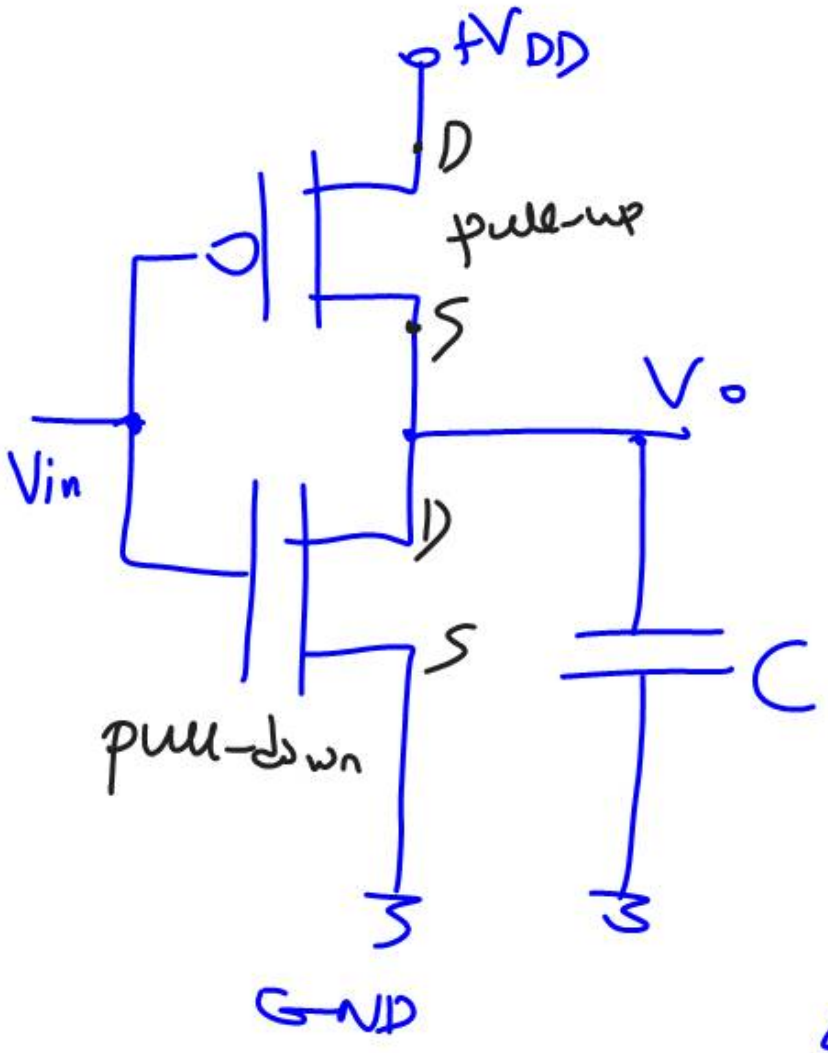


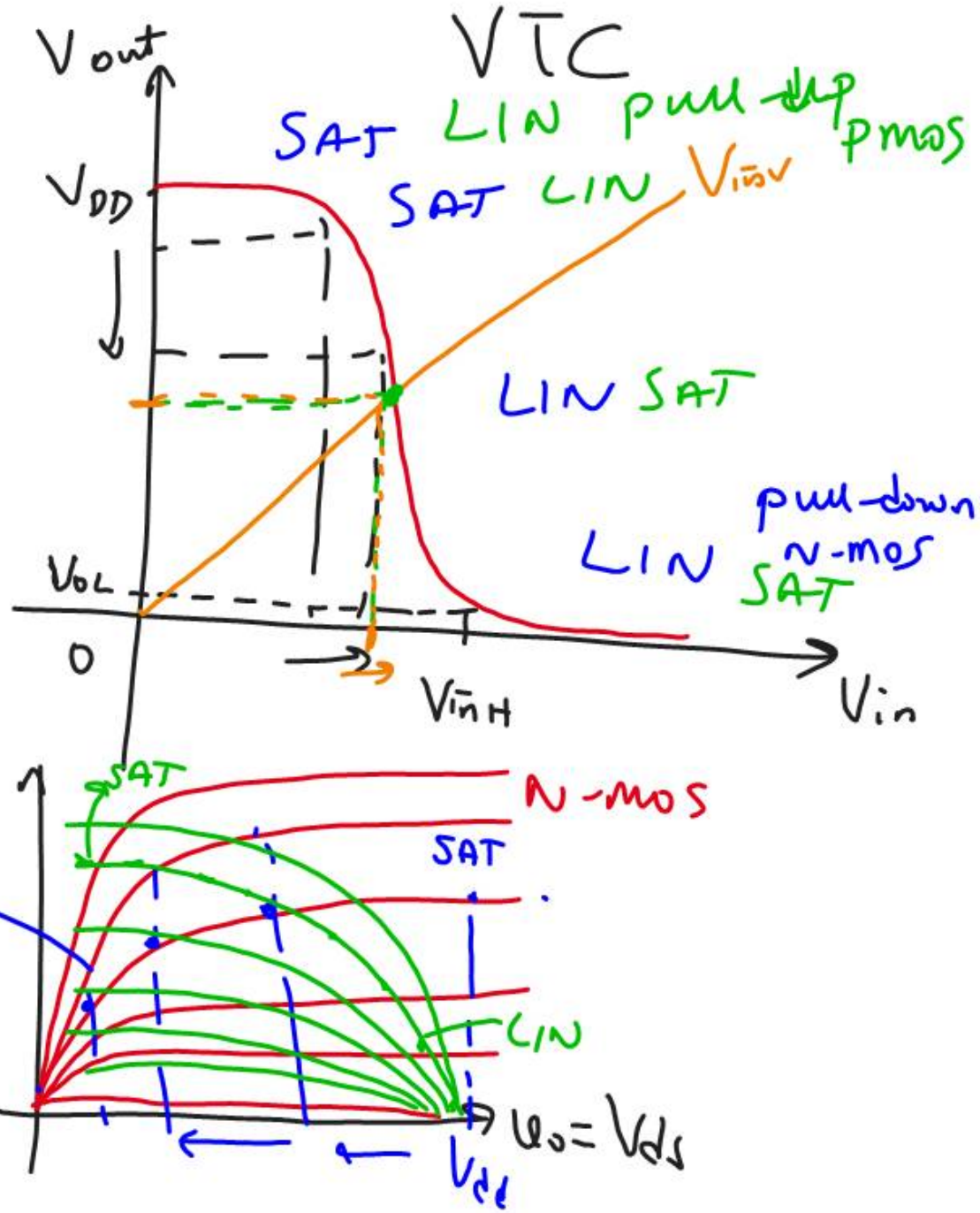




Layout of the CMOS inverter on Si


q+V_DD
X
R_pd
C
V_o
V_DD
0.5V_DD
0.69R_pdC
t
$v_o = V_{DD} e^{-t/\tau}$
$\tau = R_{pd} \cdot C$
$v_o = V_{DD} e^{-t/R_{pd}C}$
$v_o = V_{DD} e^{-0.69} = 0.5 V_{DD}$





$V_{ds\ of\ pull\ down} = V_o$

$V_{ds\ pull\text{-}up} = V_{DD} - V_o$

Energy lost during switching $= CV_{DD}^2$

Power lost $= C V_{DD}^2 \cdot f$ in a switching cycle

Memories

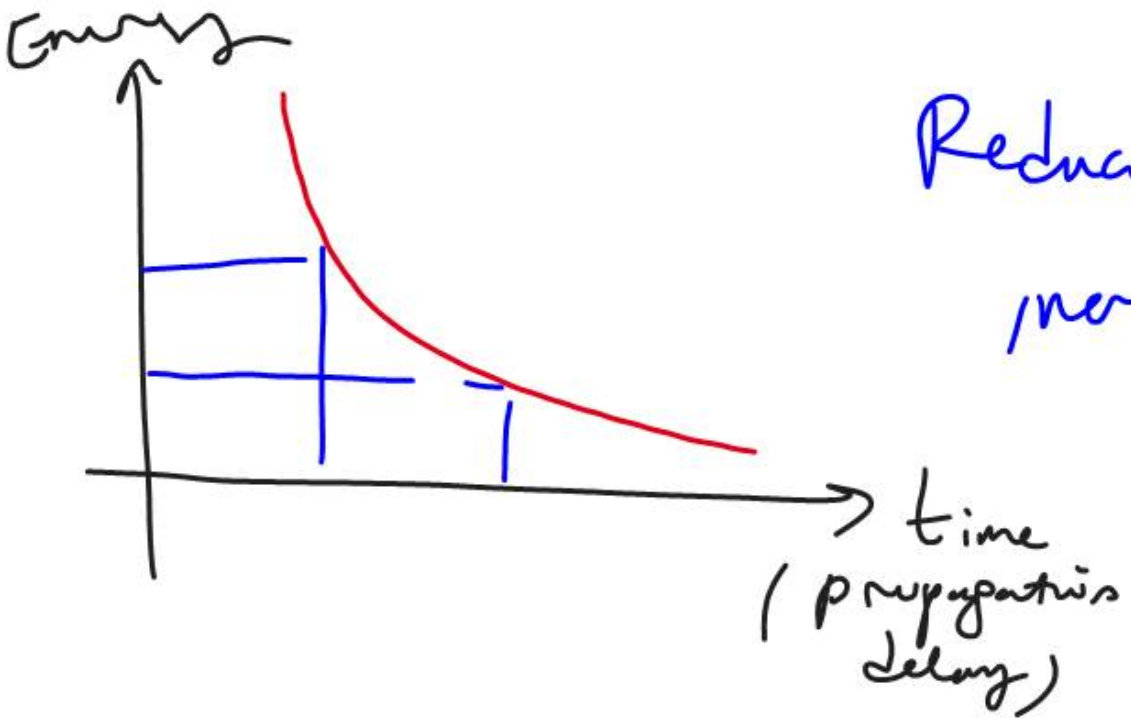
Power lost:

① Charging and Discharging transients $= CV_{DD}^2 \cdot f$ DYNAMIC

* Reduce V_{DD}
* Reduce C

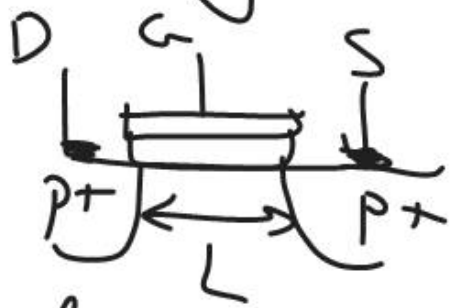
② Static power (when both transistors are ON momentarily during switching) (V_{DD} and GND are shorted/connected)

③ Leakage currents in the Inverter



Reducing V_{DD} will increase the t_{pLH} mostly.

* Reducing C $\Rightarrow$ Reducing Size of the Transistor



$$\mathcal{E} = \frac{V_{DS}}{L}$$

If we have $V_{DS} = 1\,V$

$L = 20\,nm$

$$\mathcal{E} = \frac{1}{20\times10^{-9}} = \frac{100\times10^{7}}{20} = 5\times10^{7}\ V/m$$

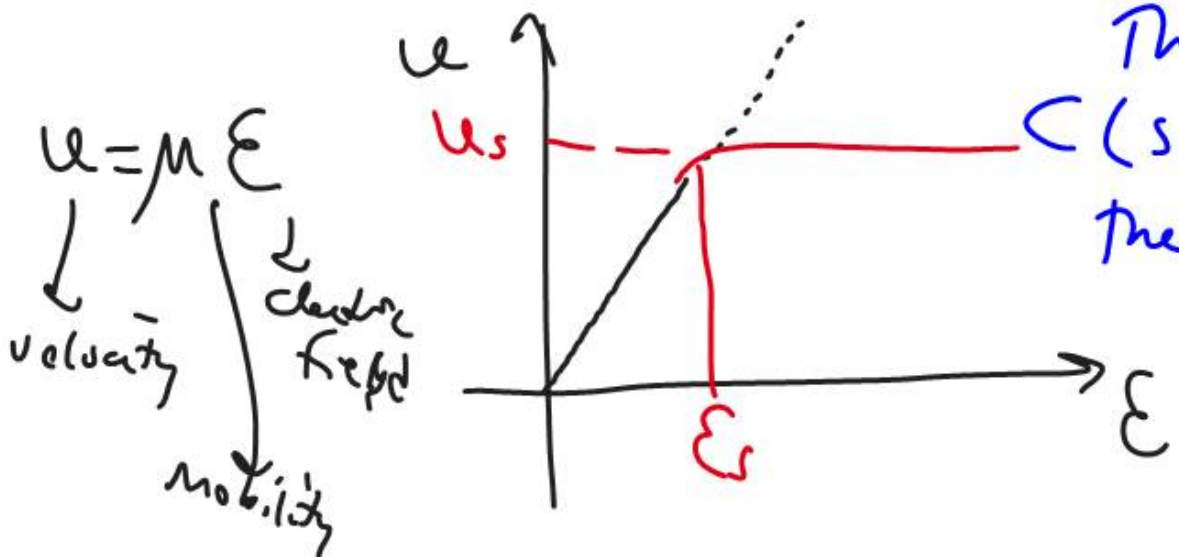
$\mathcal{E} = 5 \times 10^7 \, V/m = 5 \times 10^5 \, V/cm = 500 \, kV/cm$!!

$$\frac{V}{m} \cdot \frac{1\,m}{100\,cm}$$

The carriers in the channel will feel this $\mathcal{E}$!

This will saturate the carrier speed.

High FIELDS → Short channel Effect!



The benefits of reducing C (size), will be limited by the short channel effects this time.

HW = What is the Logical Effort?

Explain.