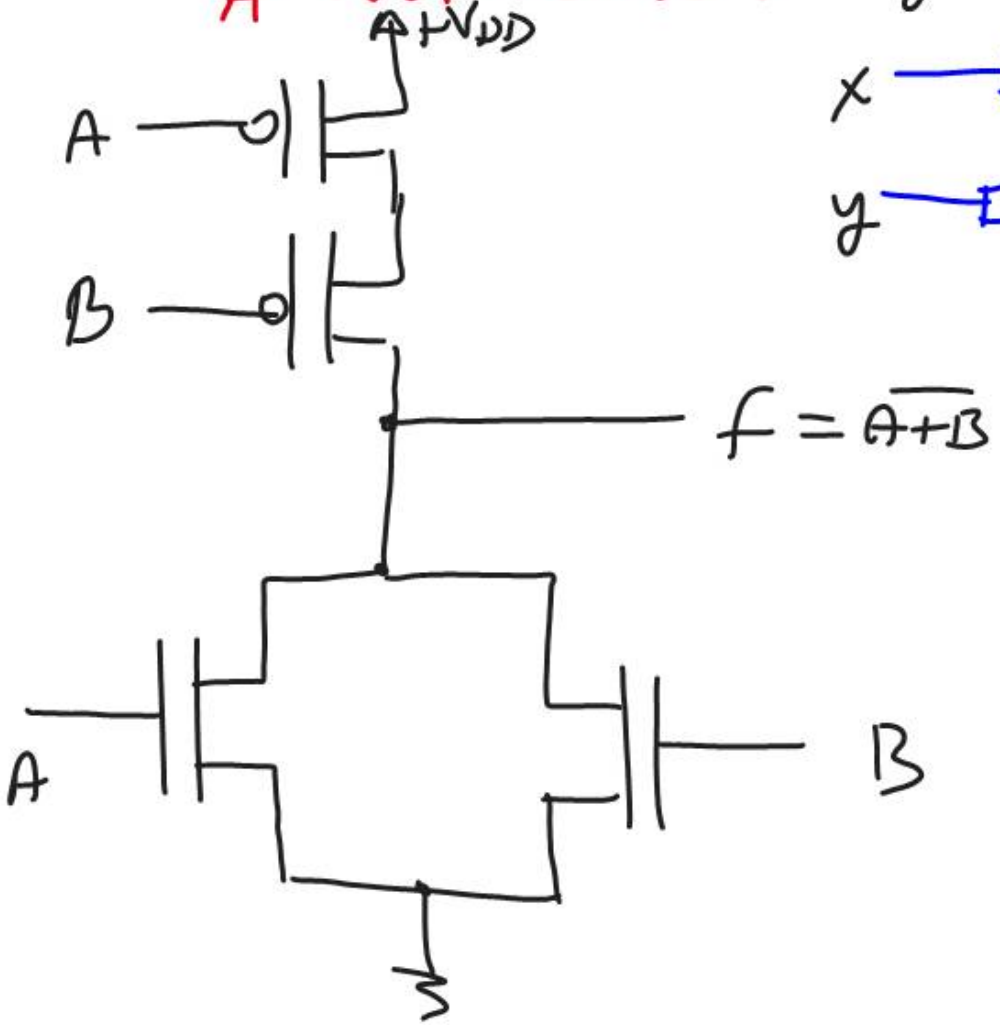
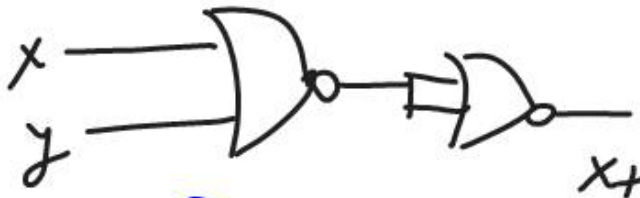
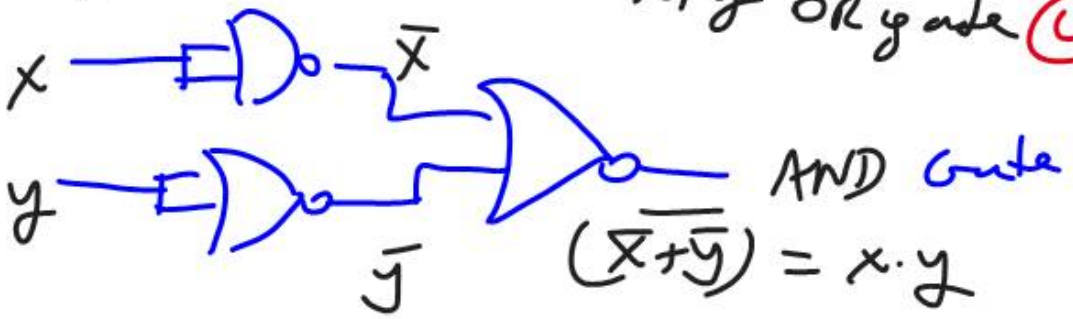
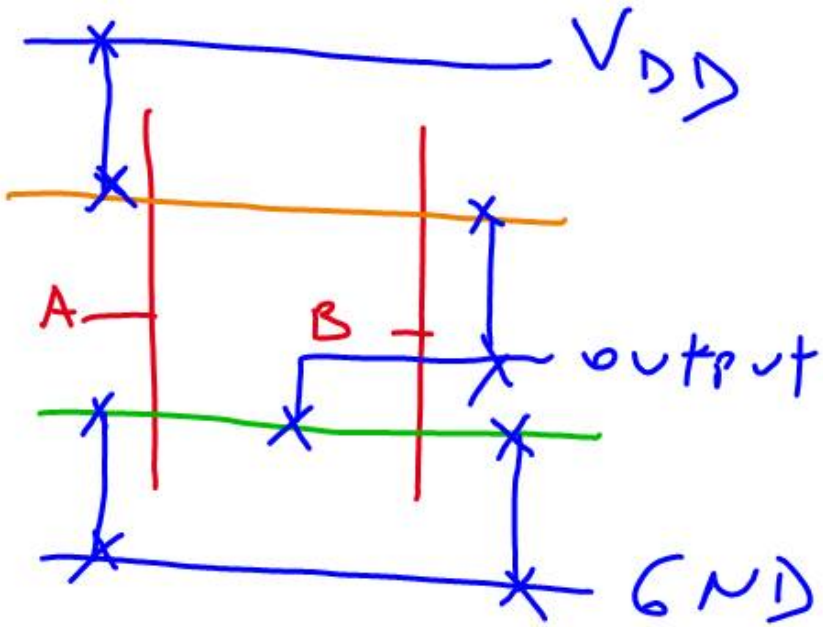
10 Dec 2010

A NOR Gate :

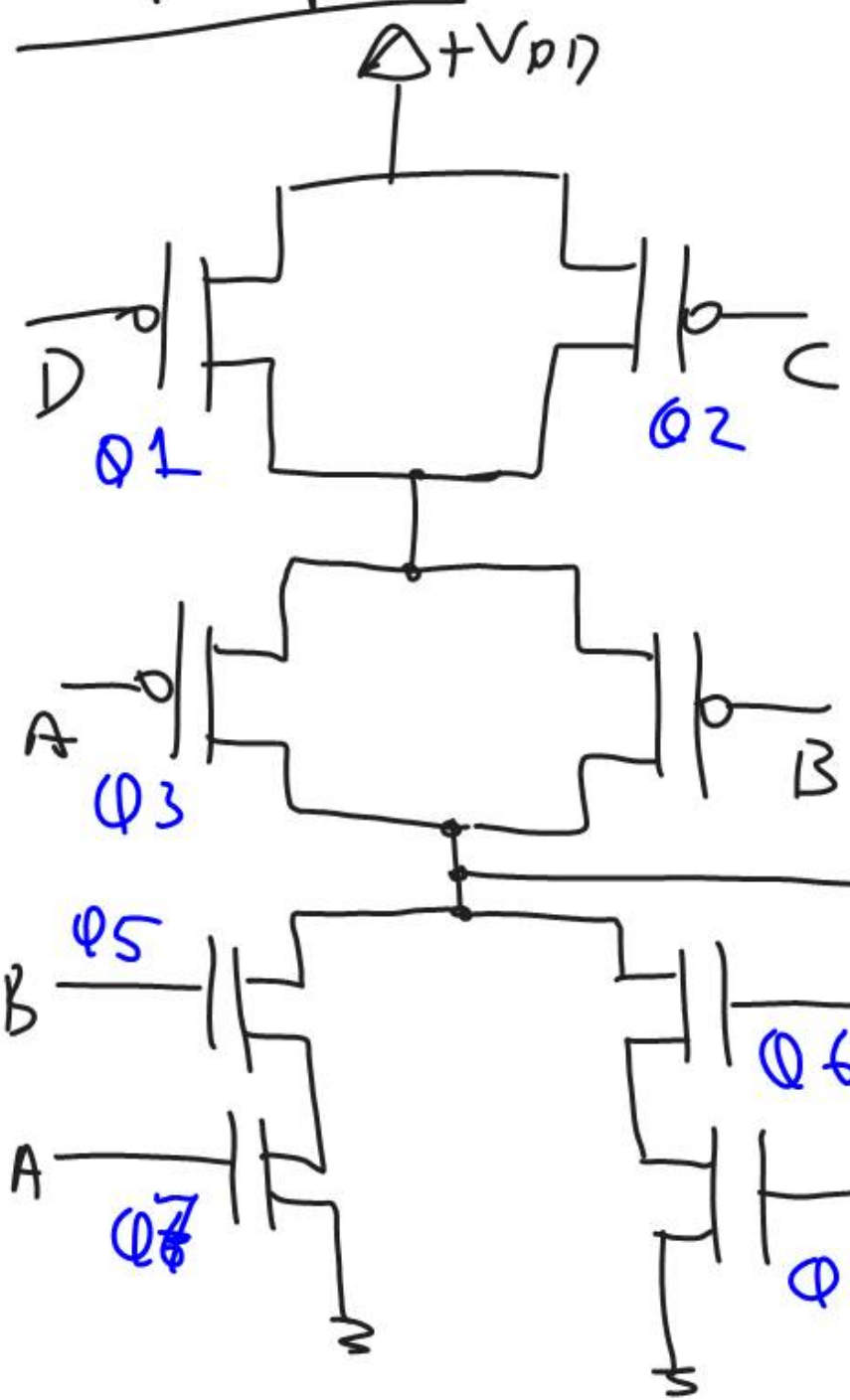




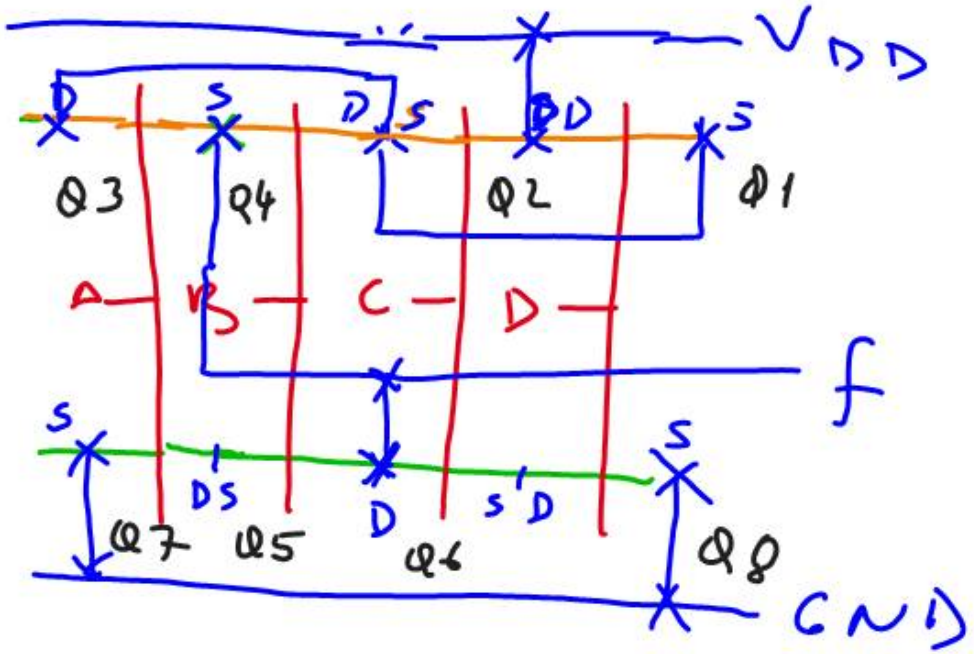


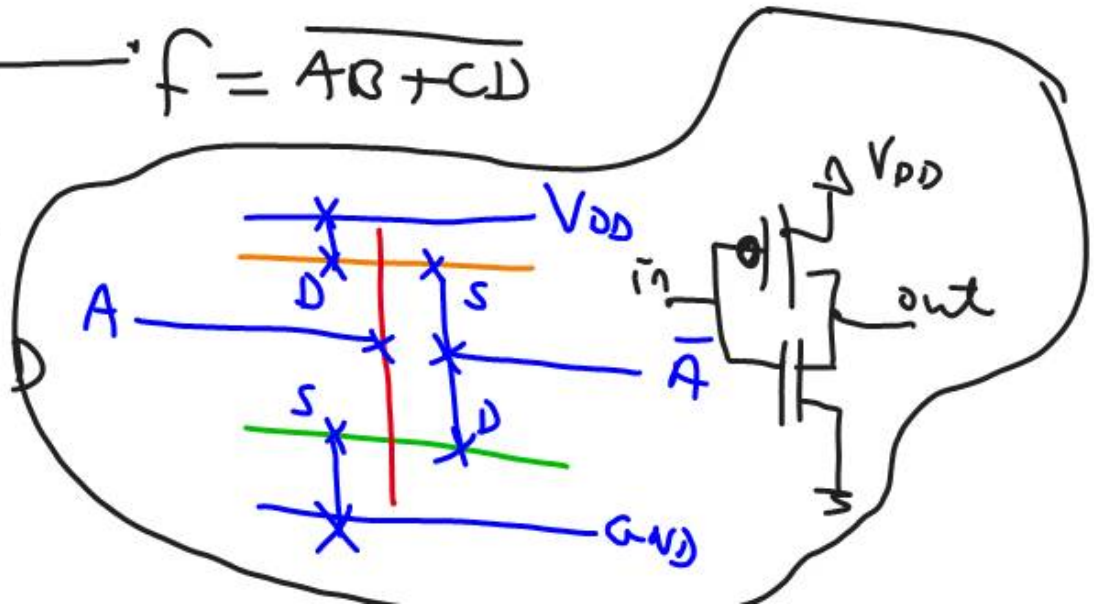


example:



Stick Diagram

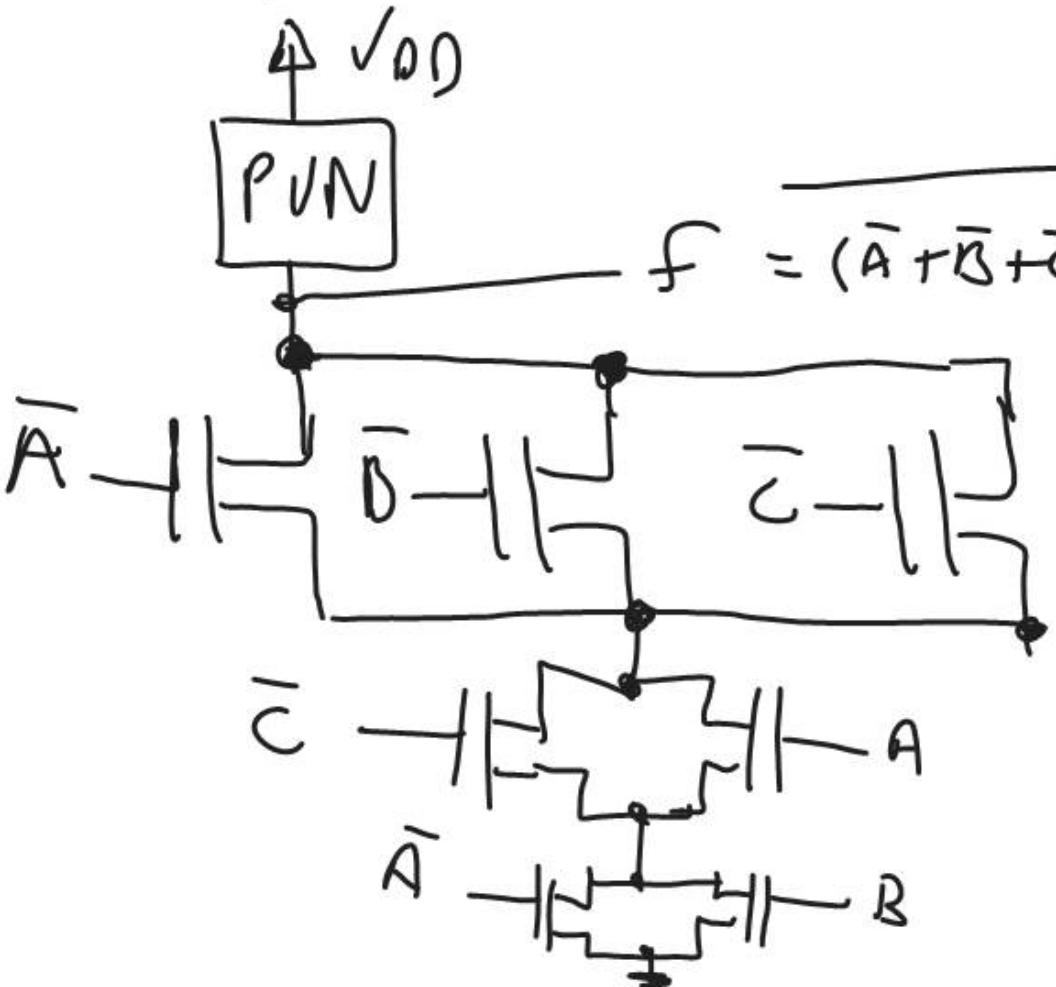




$$f = ABC + C\bar{A} + A\bar{B}$$

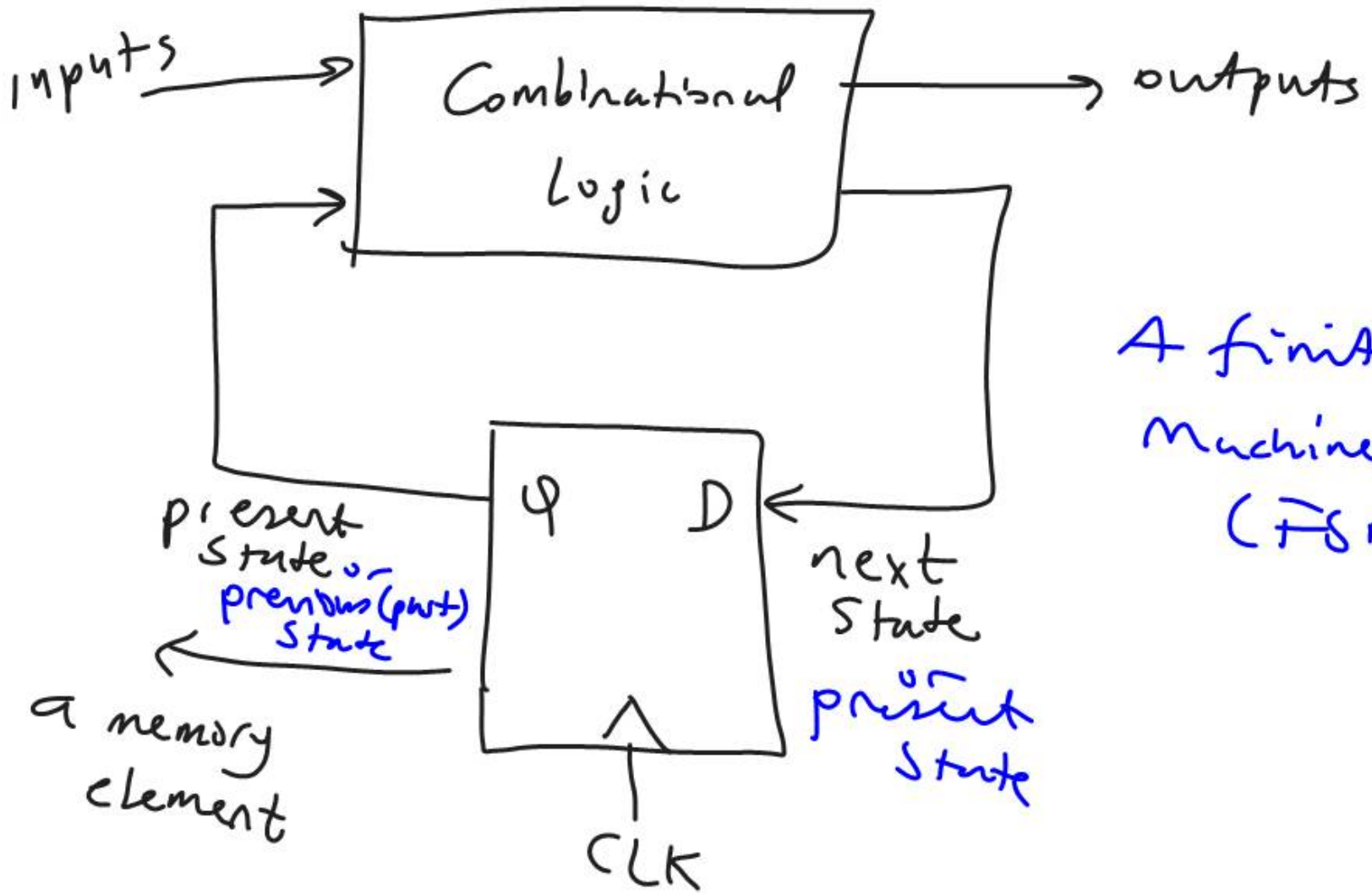
$$PDN = \bar{f} = (\overline{ABC}) \cdot (\overline{C\bar{A}}) \cdot (\overline{A\bar{B}})$$

$$= (\bar{A} + \bar{B} + \bar{C})(\bar{C} + A) \cdot (\bar{A} + B)$$



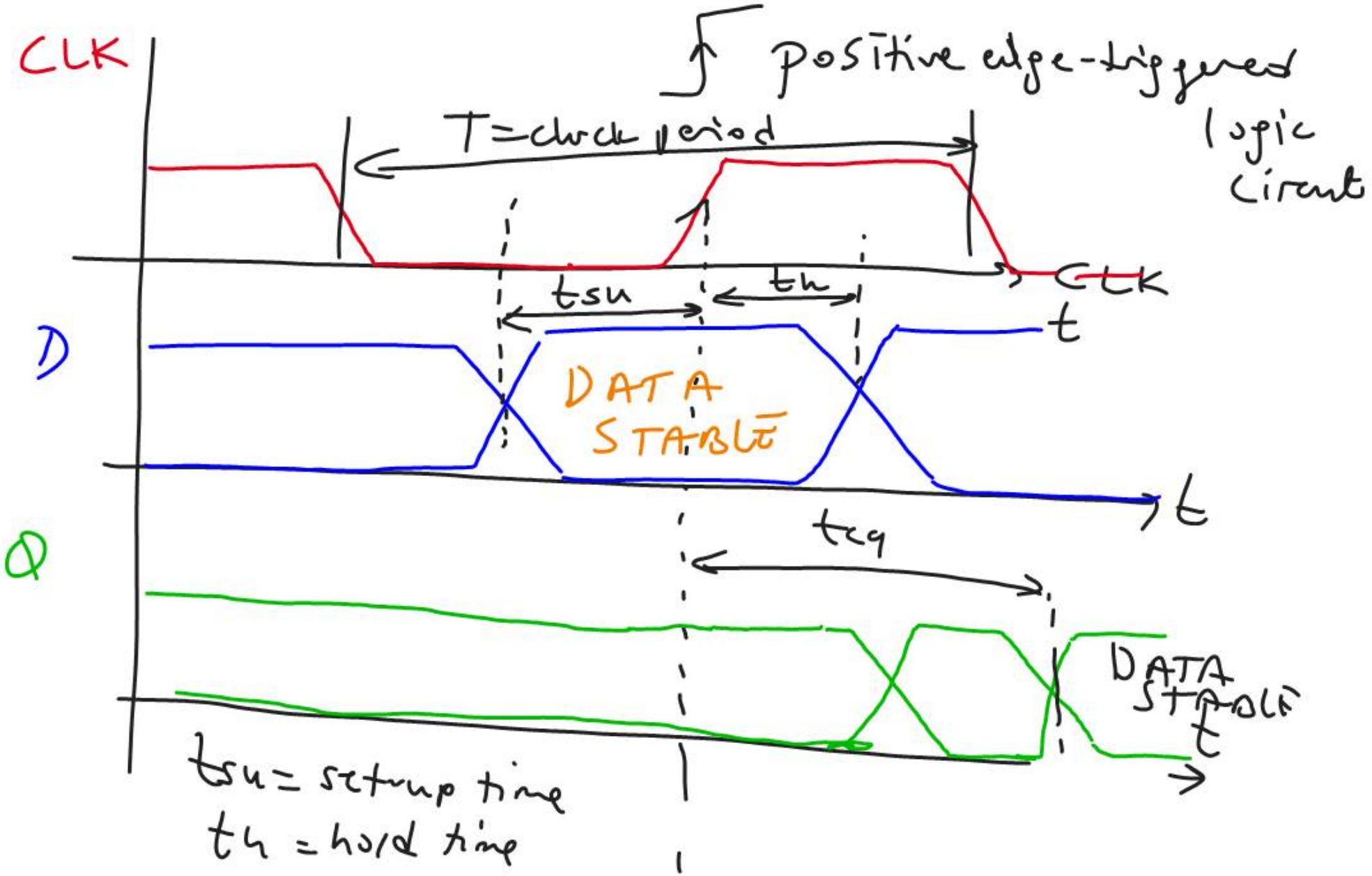
$$f = \overline{(\bar{A} + \bar{B} + \bar{C})(\bar{C} + A)(\bar{A} + B)} = ABC + C\bar{A} + A\bar{B}$$

SEQUENTIAL LOGIC CIRCUITS



A finite State Machine (FSM)

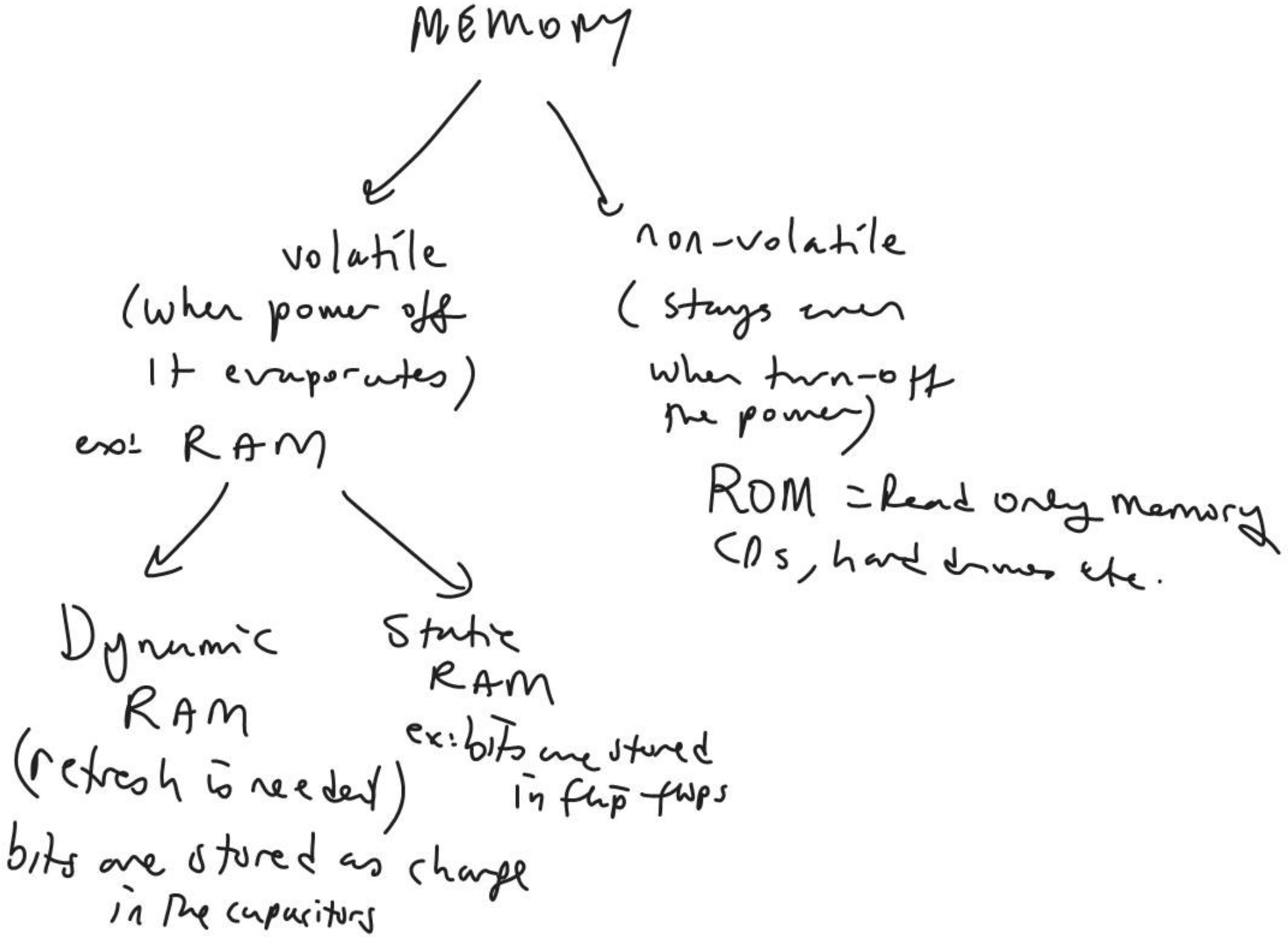
Timing Metrics for Sequential Circuits



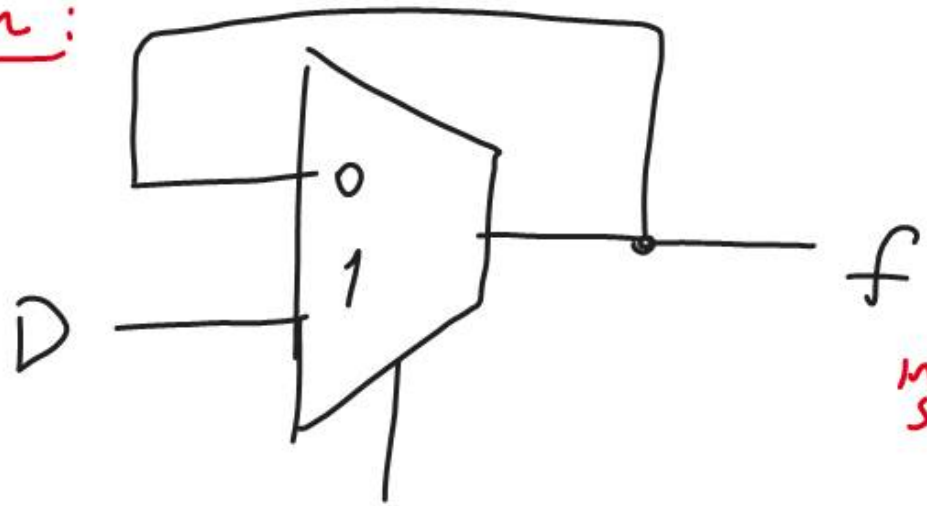
The clock period T, at which the sequential circuit operates, must accomodate the longest delay of any stage in the network.

Assume the delay (total) of the combinatorial circuits is t_{plogic}

$$T \geq t_{c-q} + t_{plogic} + t_{su}$$

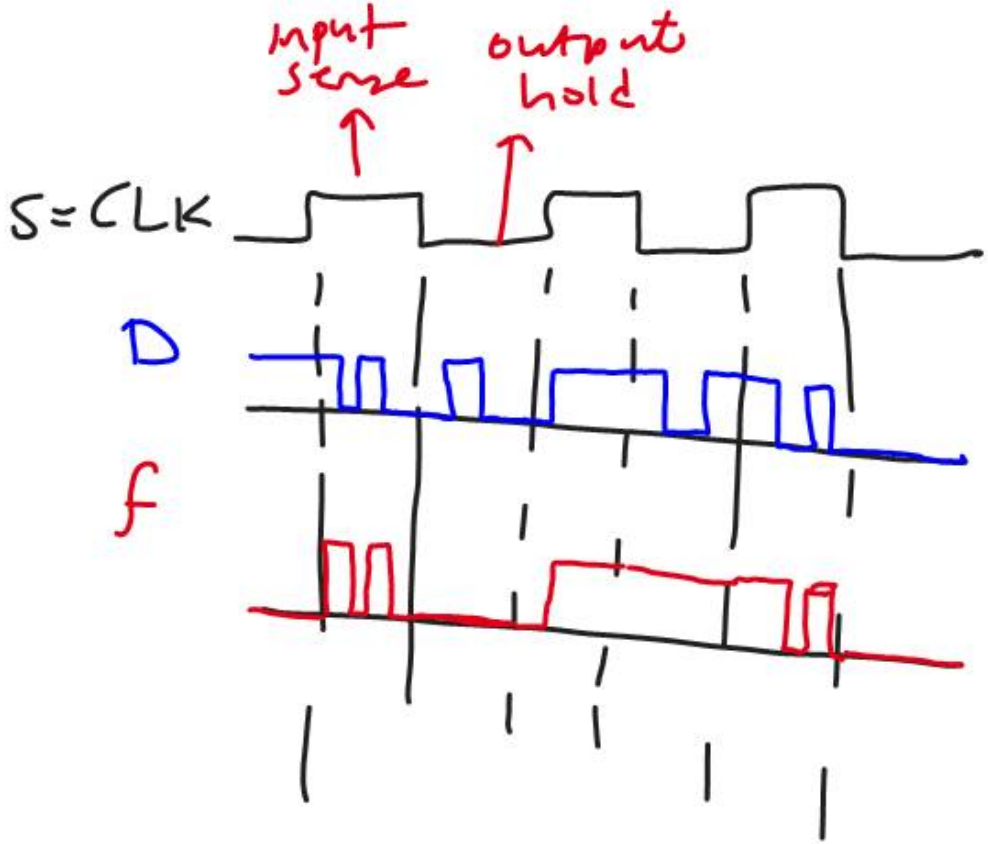

MEMORY
volatile
(when power off
it evaporates)
non-volatile
(stays even
when turn-off
the power)
ex: RAM
ROM = Read only memory
CDs, hard drives etc.
Dynamic
RAM
(refresh is needed)
bits are stored as charge
in the capacitors
Static
RAM
ex: bits are stored
in flip flops

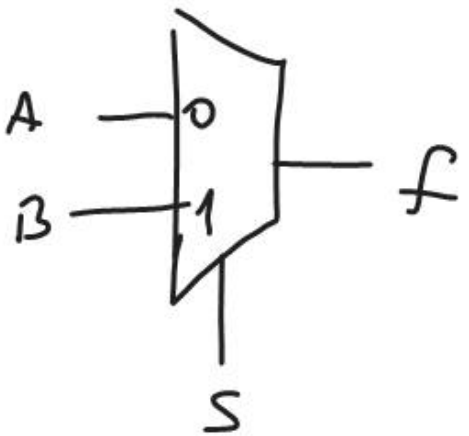
A Latch:

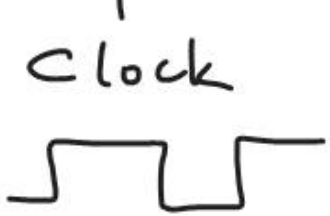


a positive Latch

It senses the input when the CLK is HIGH



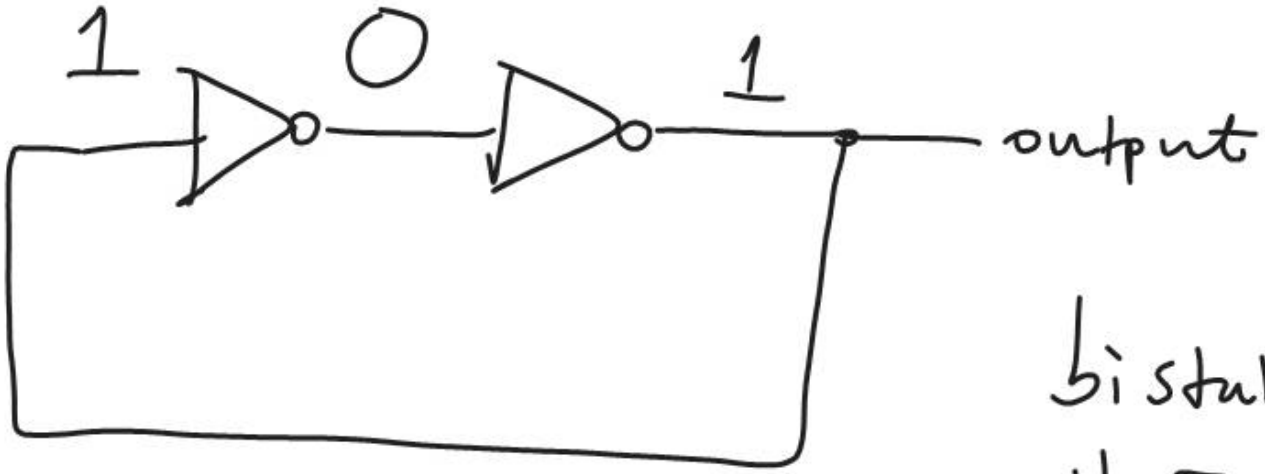




a 2-to-1 multiplexer (MUX)

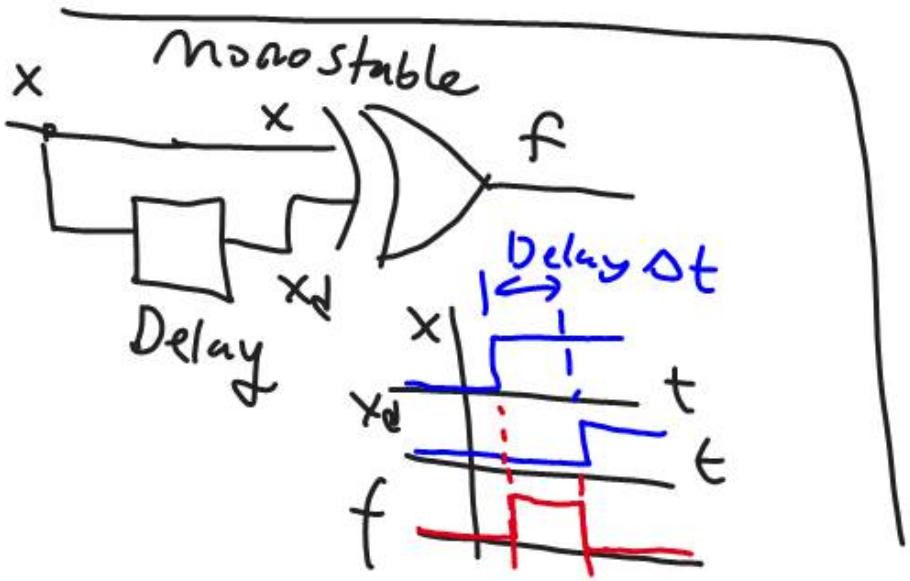
S	f
0	A
1	B

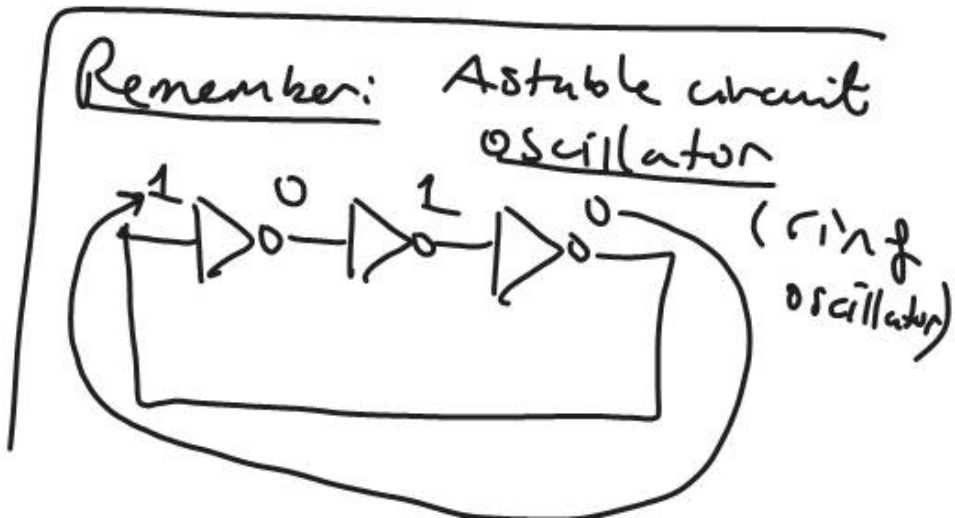
STATIC LATCHES and REGISTERS



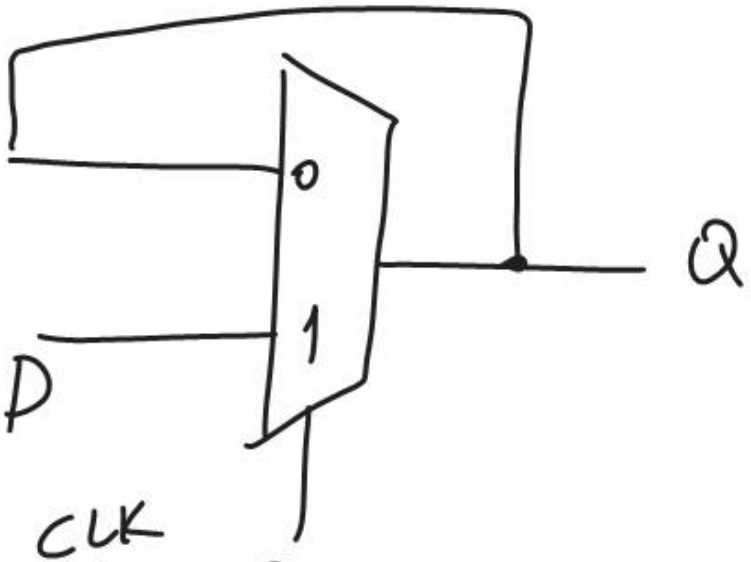
bistable circuit
It is a memory element.
It keeps 1 bit of data.

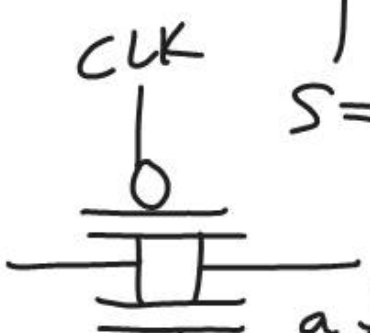
a bistable ≡ a flip-flop





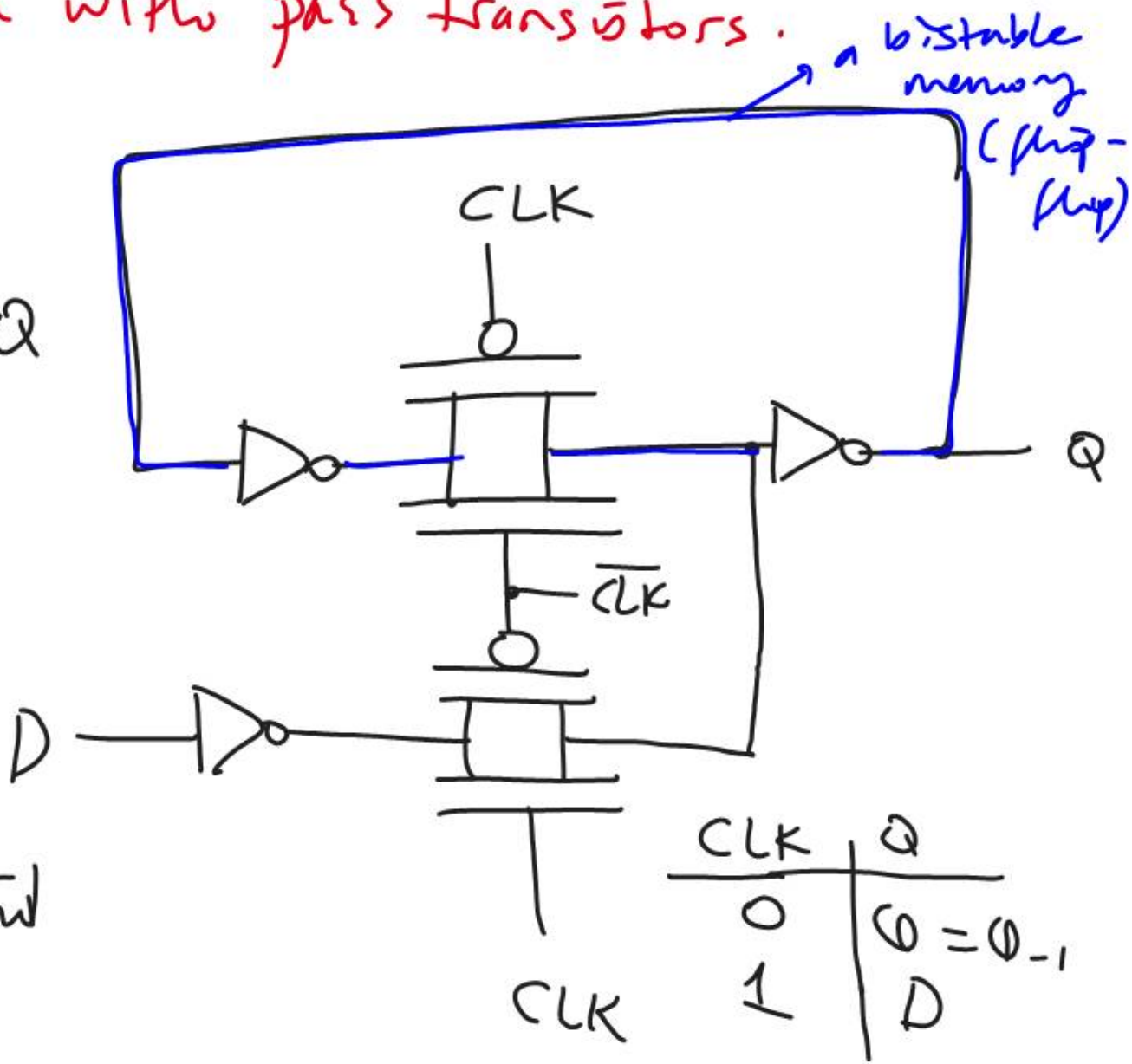
A positive Latch with pass transistors.





We use N-MOS and PMOS transistors.

4 transistors (3 inverters)

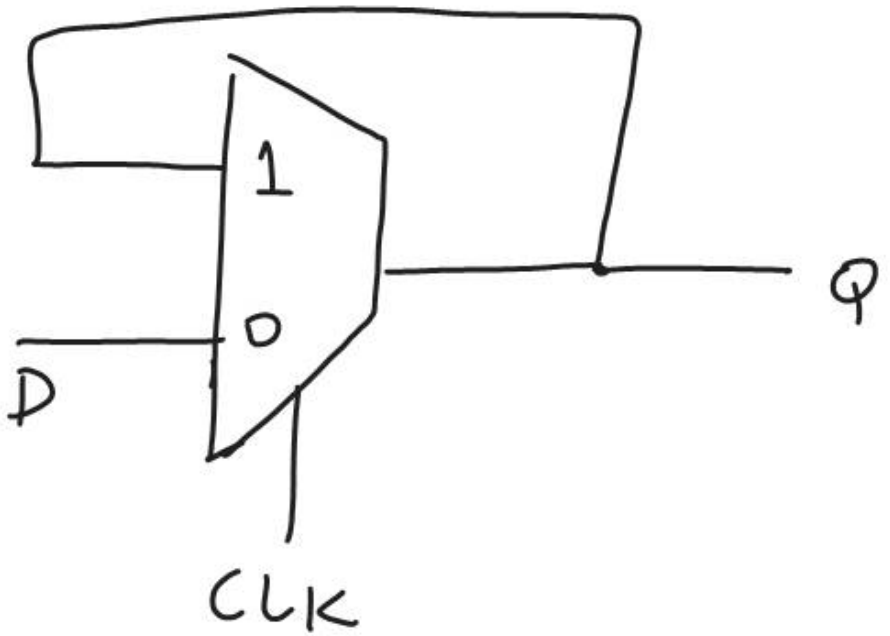


CLK	Q
0	$Q = Q_{-1}$
1	D

When CLK = 1 D is passed at output

When CLK = 0 then previous Q is kept

A negative latch

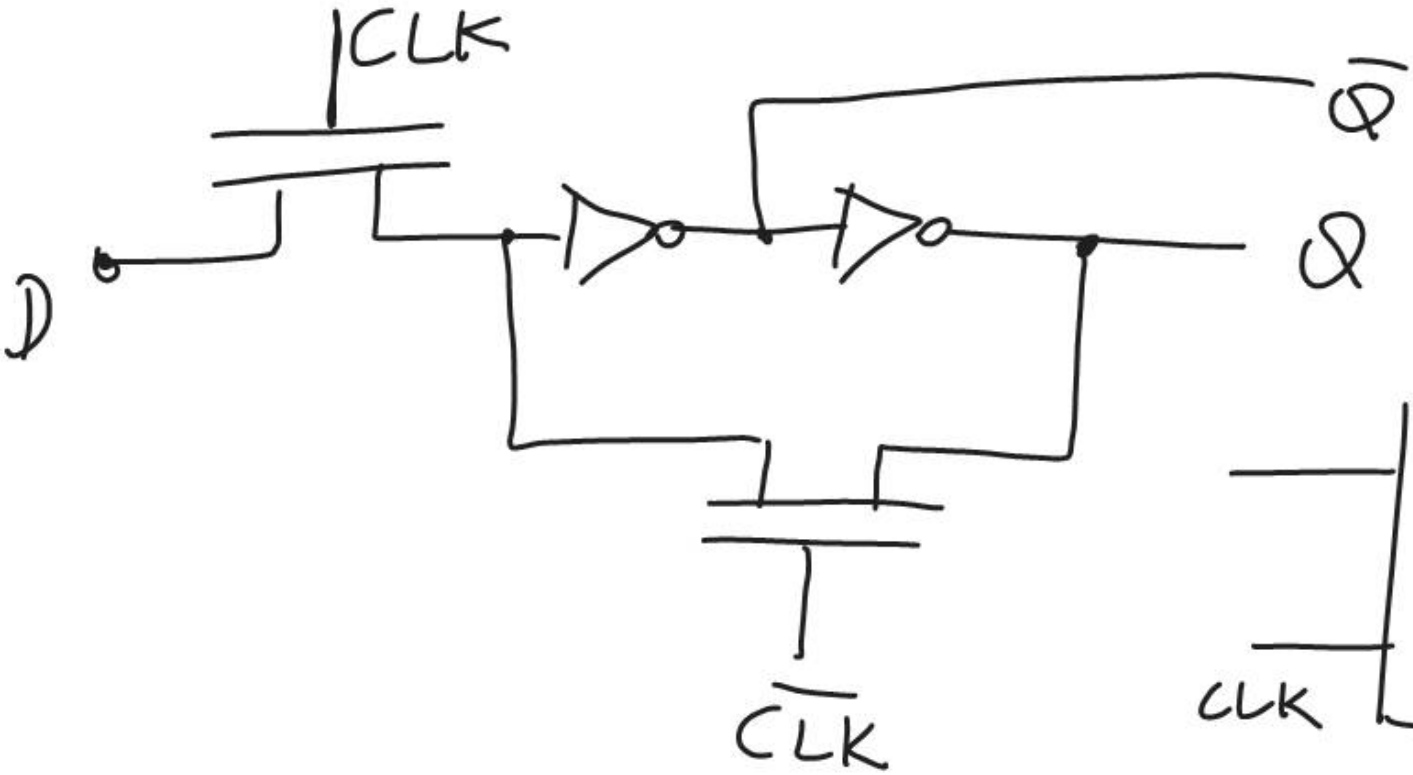


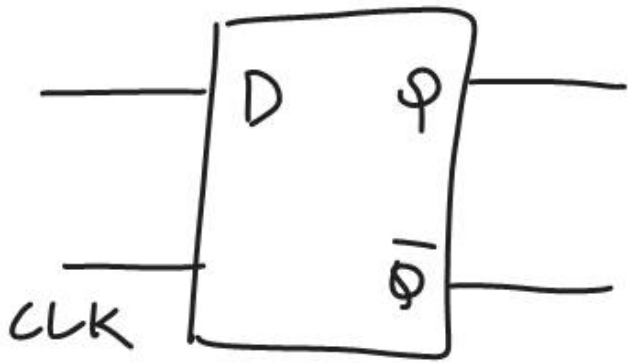
it senses when CLK low

it holds when CLK HIGH

In these latches when configured as in the previous page has 4 transistors (in the transmission gates 4 transistors)

A CLK should drive these 4 transistors. # of transistors should be reduced.



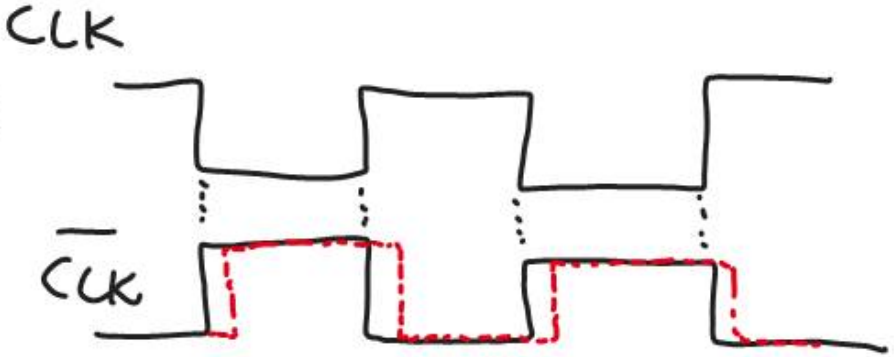


a D-Latch

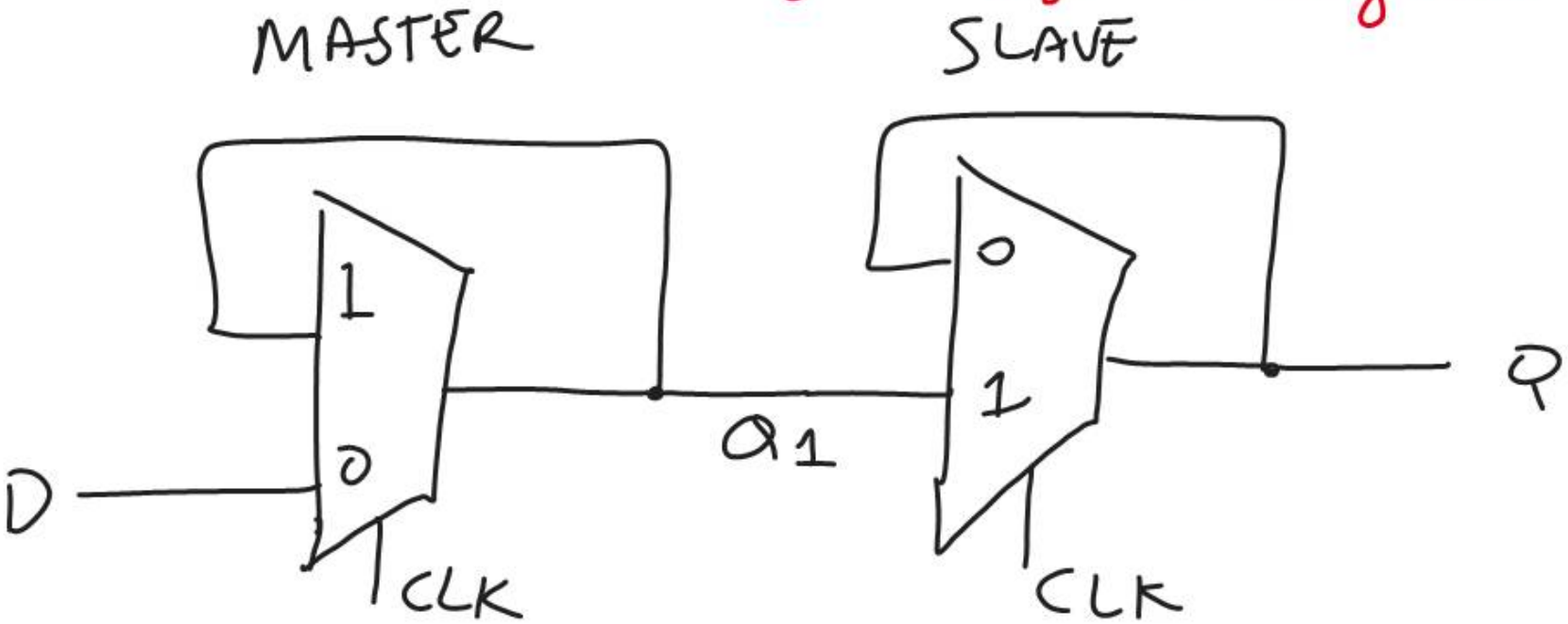
This circuit is better:

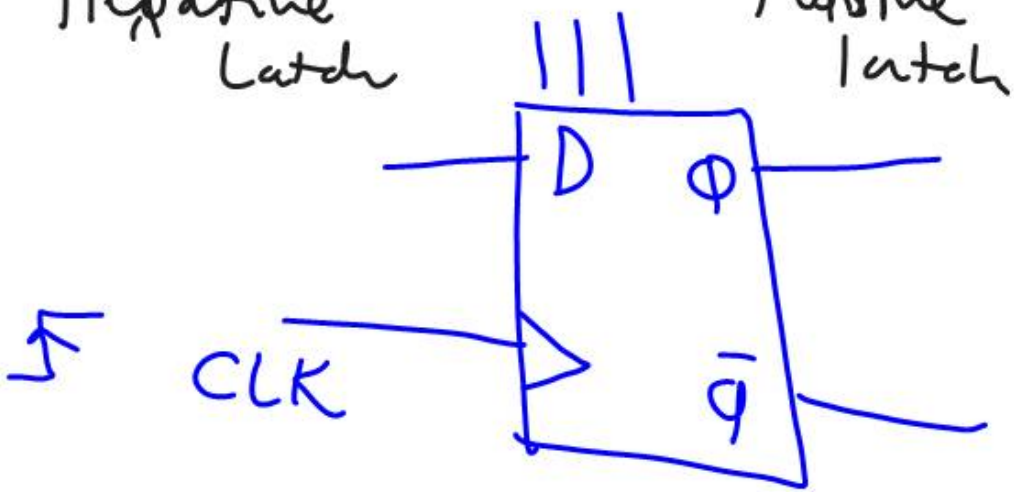
- It has 2 transistors
- Both are nMOSs.

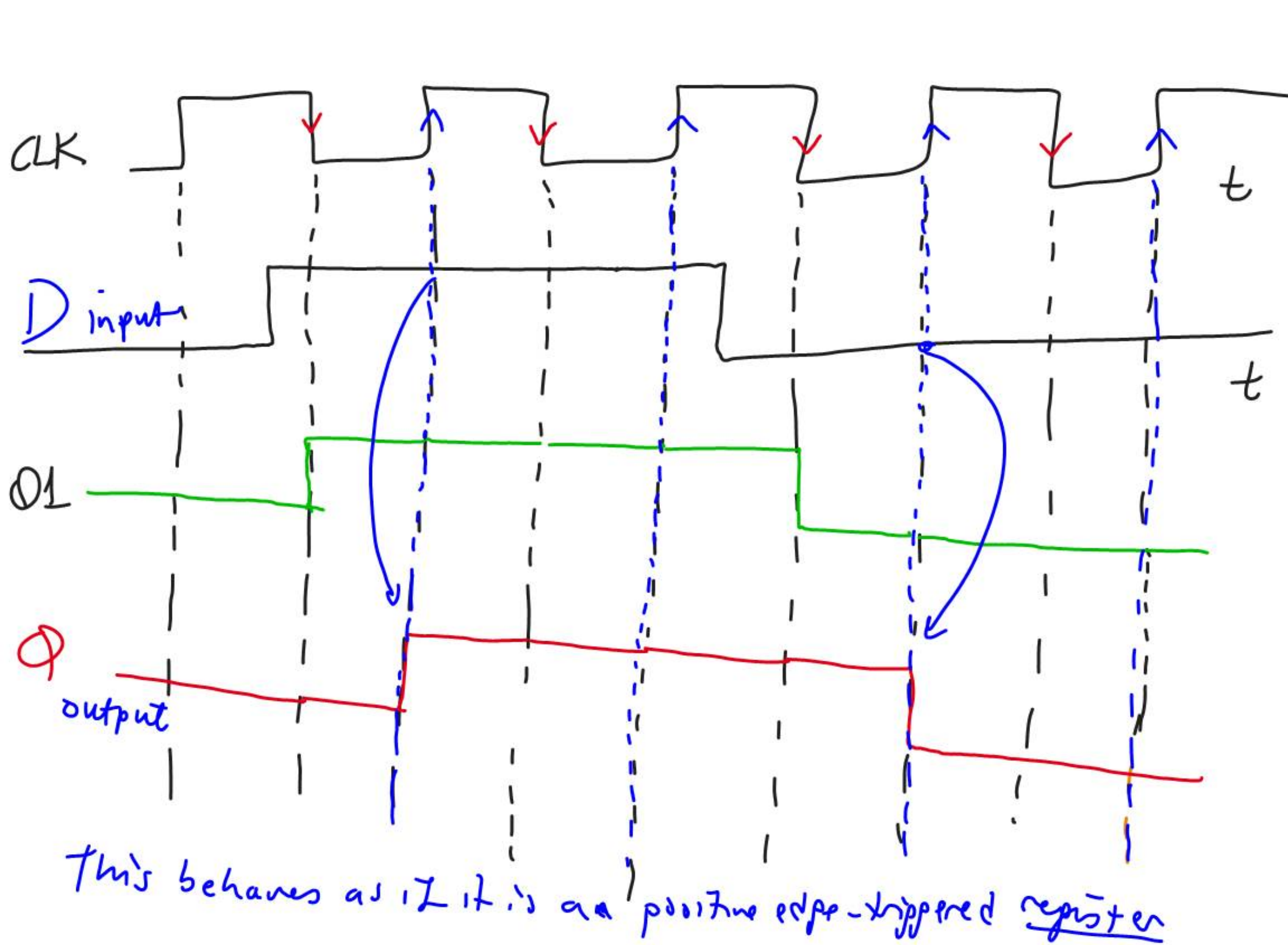
CLK drives 2 transistors.



A Master-Slave Edge-Triggered Register







This behaves as if it is a positive edge-triggered register