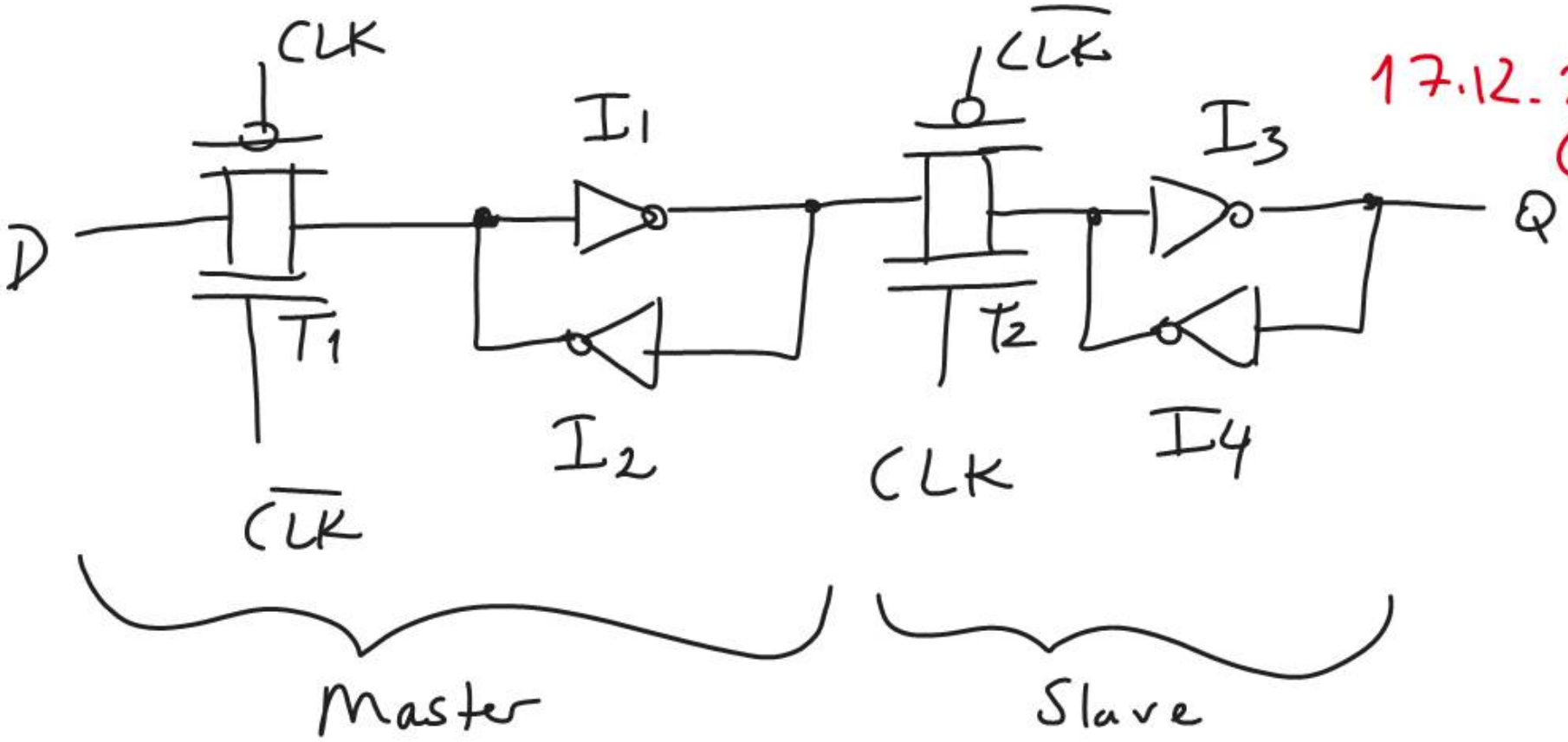
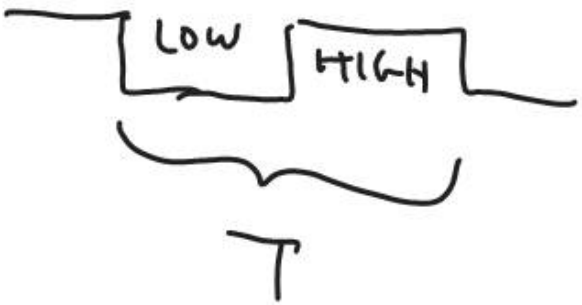
17.12.2010

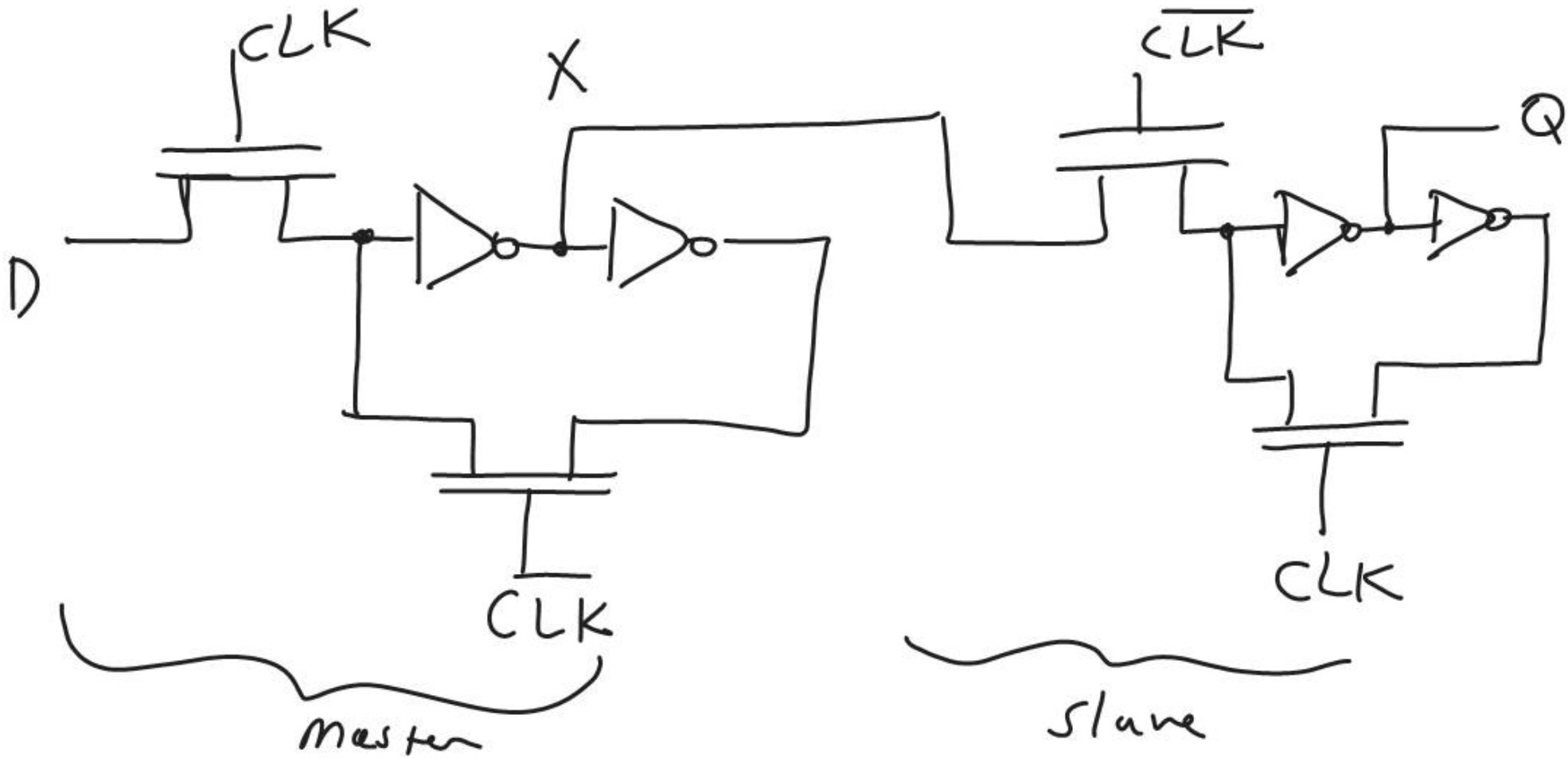


CLK → LOW ⇒ T1 ON T2 OFF D is sensed

CLK → ~~LOW~~ HIGH ⇒ T1 OFF T2 ON sensed D is transferred to output Q



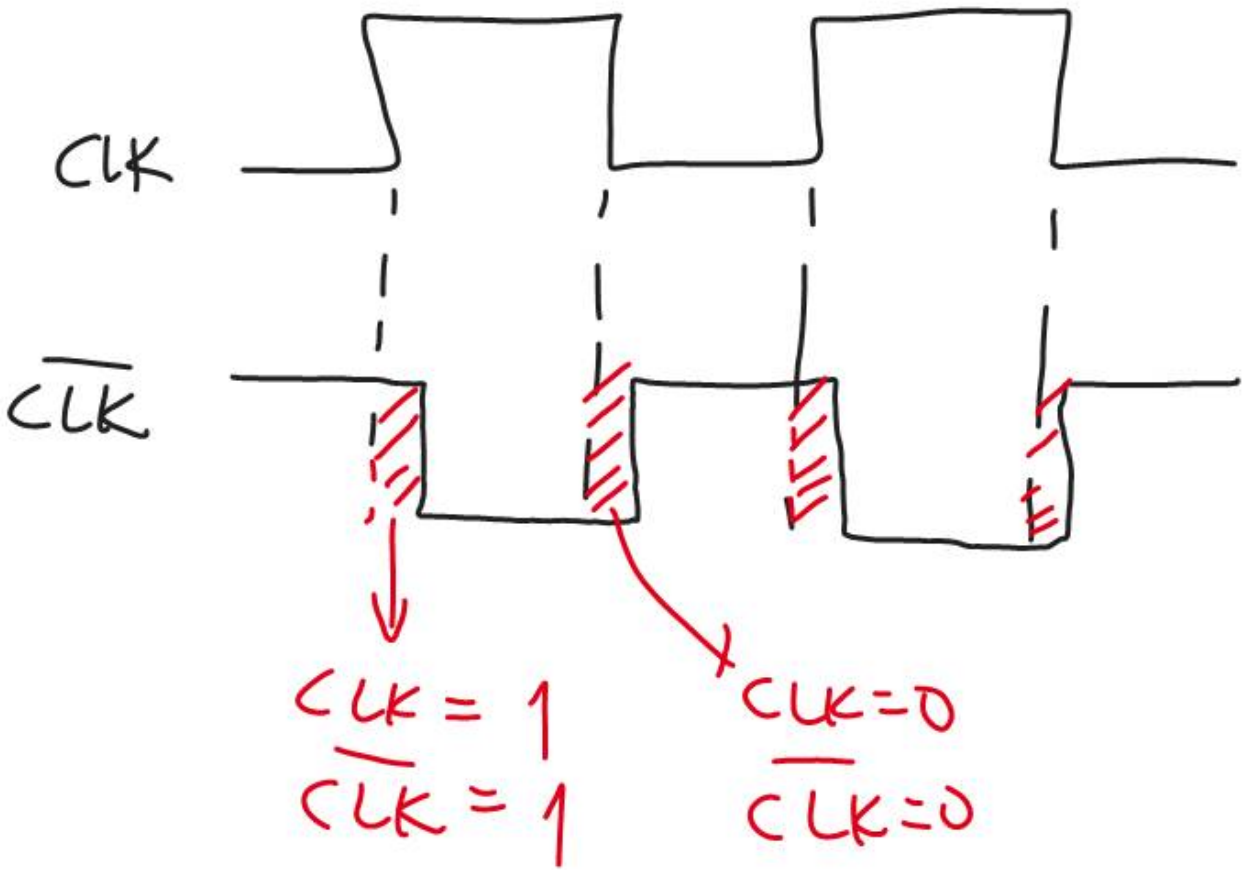
another circuit: (no transmission gate, NMOS only)



CLK → HIGH ⇒ D is sensed $X = \overline{D}$

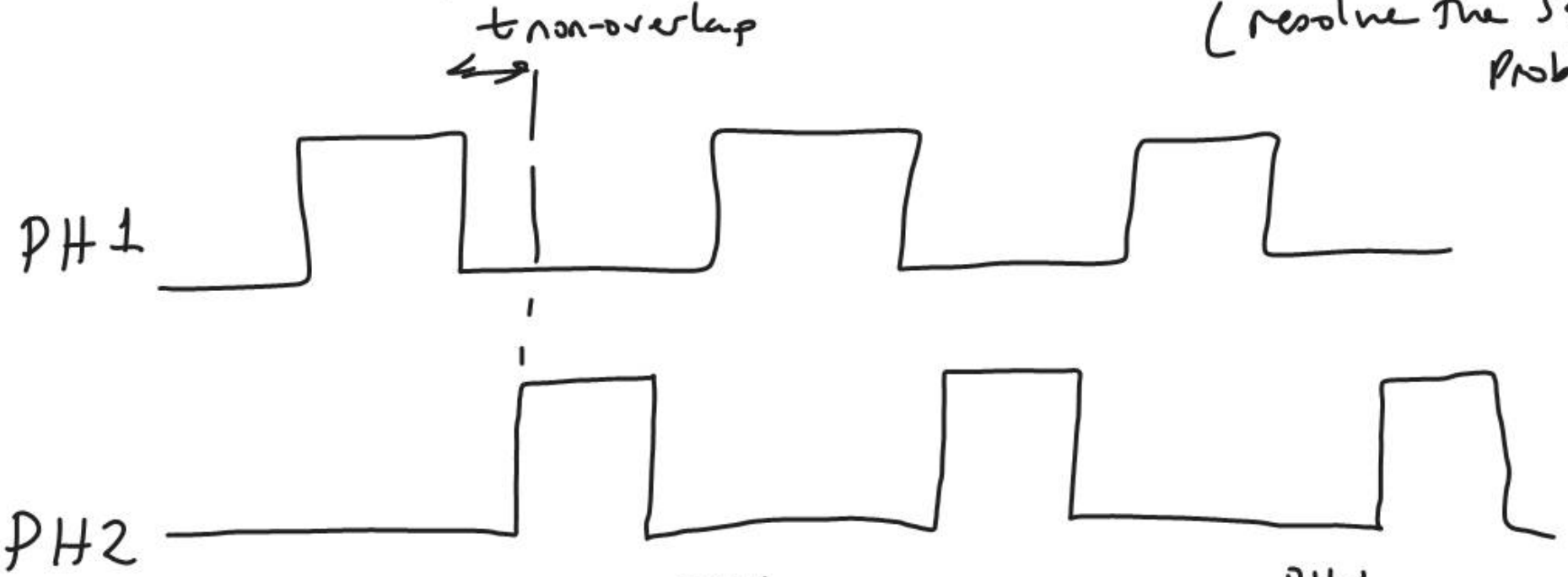
CLK → LOW ⇒ X is sensed $Q = \overline{\overline{D}} = D$

These circuits suffer also from non-ideal CLK signal. Such as:



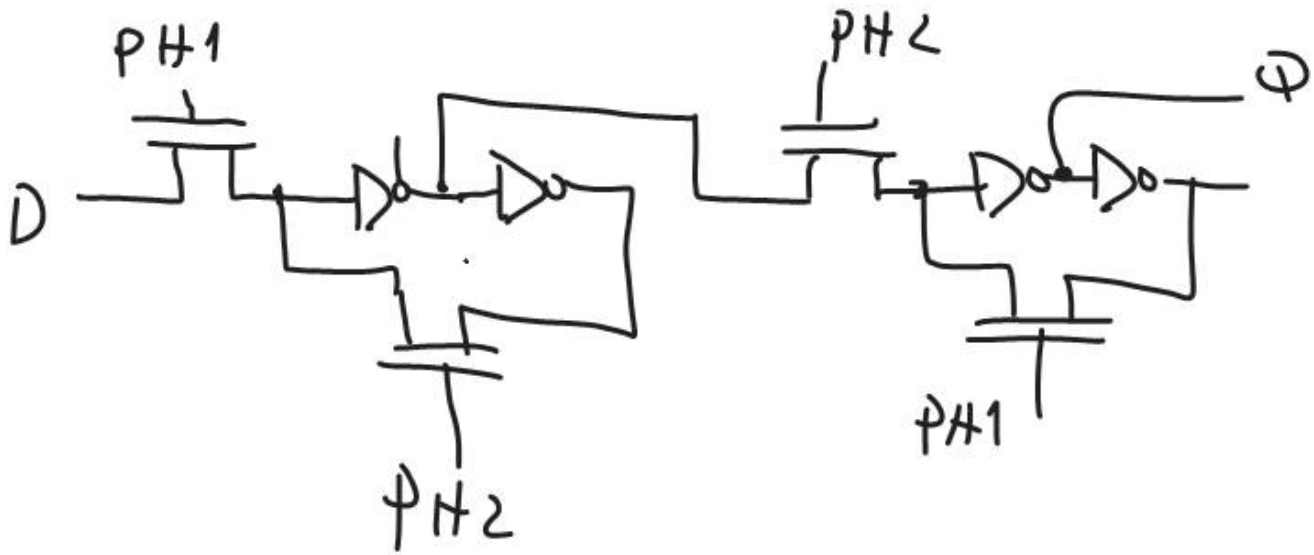
Soluzione 1:

Generate 2 independent clock signals (resolve the SKEW problem)



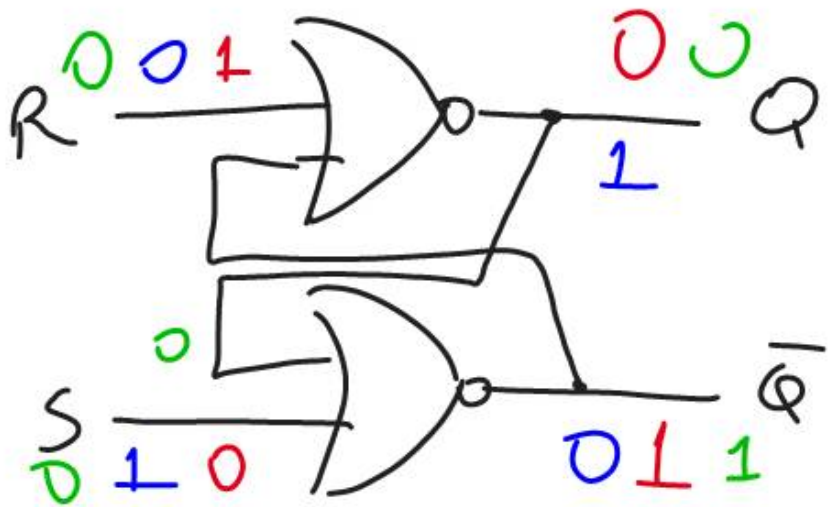
$CLK \Rightarrow PH1$

$\overline{CLK} \Rightarrow PH2$



STATIC MEMORY ELEMENT (SR flip flop)

register



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

S	R	Q
0	0	Q_{-1}
0	1	0
1	0	1
1	1	UNDEFINED

When Q is zero

① if S = 1, R = 0

Q = 1 (SET)

② if S = 0, R = 1

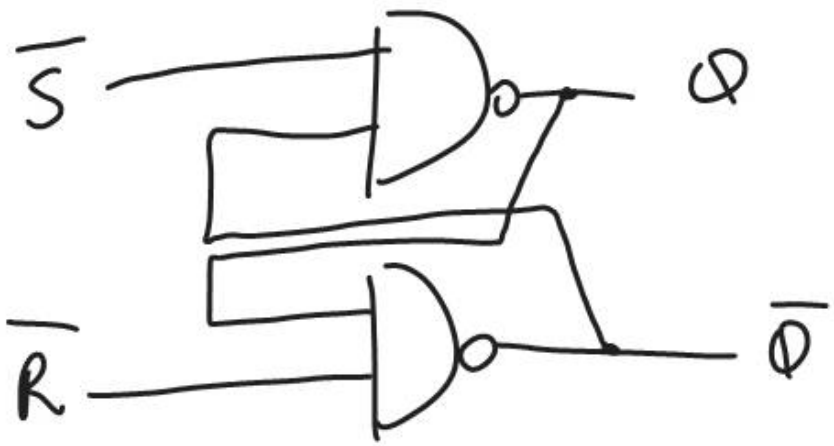
Q = 0 (RESET)

③ R = 0, S = 0

$Q = Q_{-1}$

④ R = 1, S = 1

Invalid!



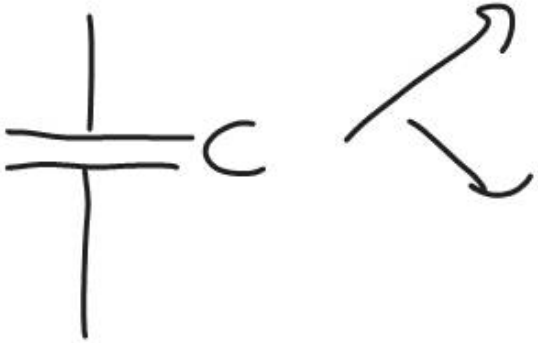
These circuits are asynchronous!

(no clock signal)

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	Invalid	

No change
$Q = Q_{-1}$

DYNAMIC LATCHES & REGISTERS



When there is charge ⟹ State ⇒ HIGH

When ≠ ; NO charge ⇒ State ⇒ LOW

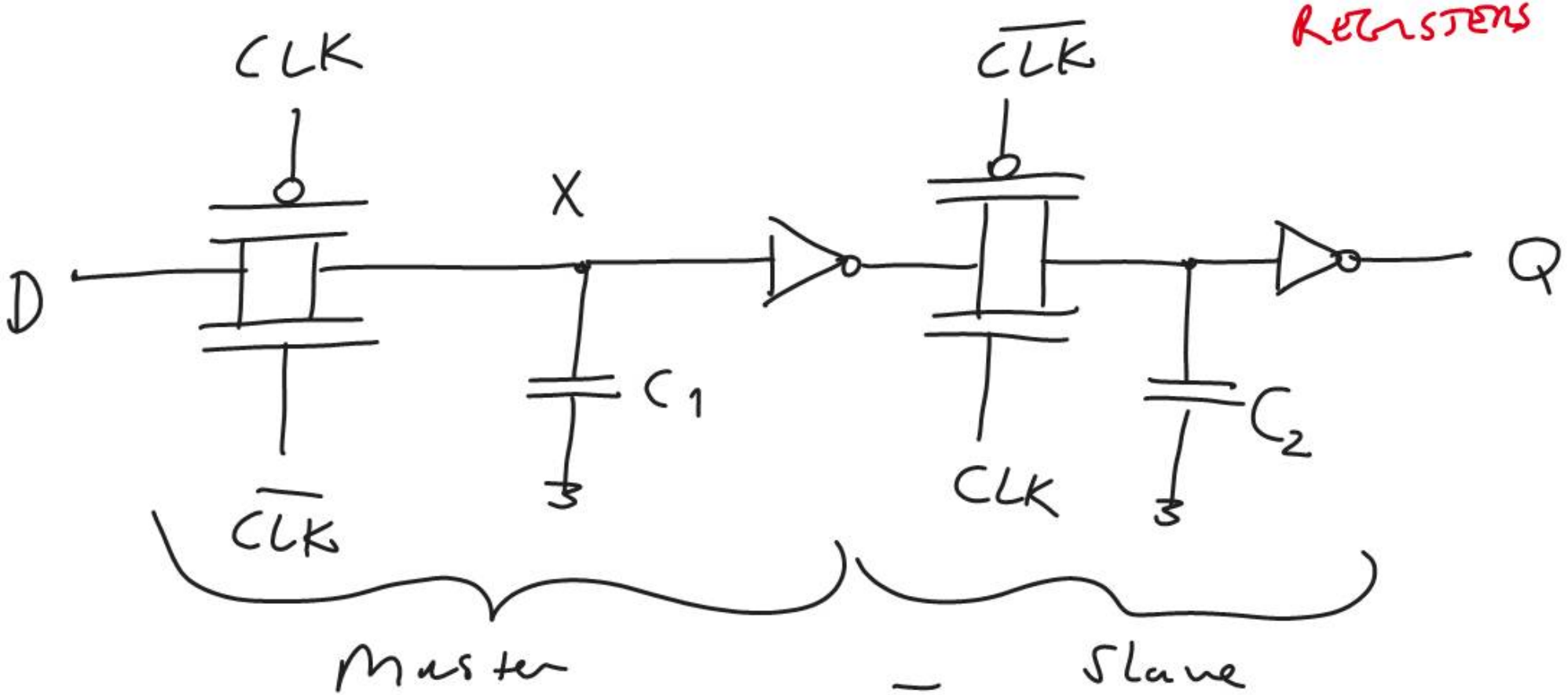
each capacitor has a leakage of charge

Therefore to keep the charge at the same level it should be periodically refreshed

When the memory element is formed by a capacitor, then we have a dynamic memory. (RAMS)

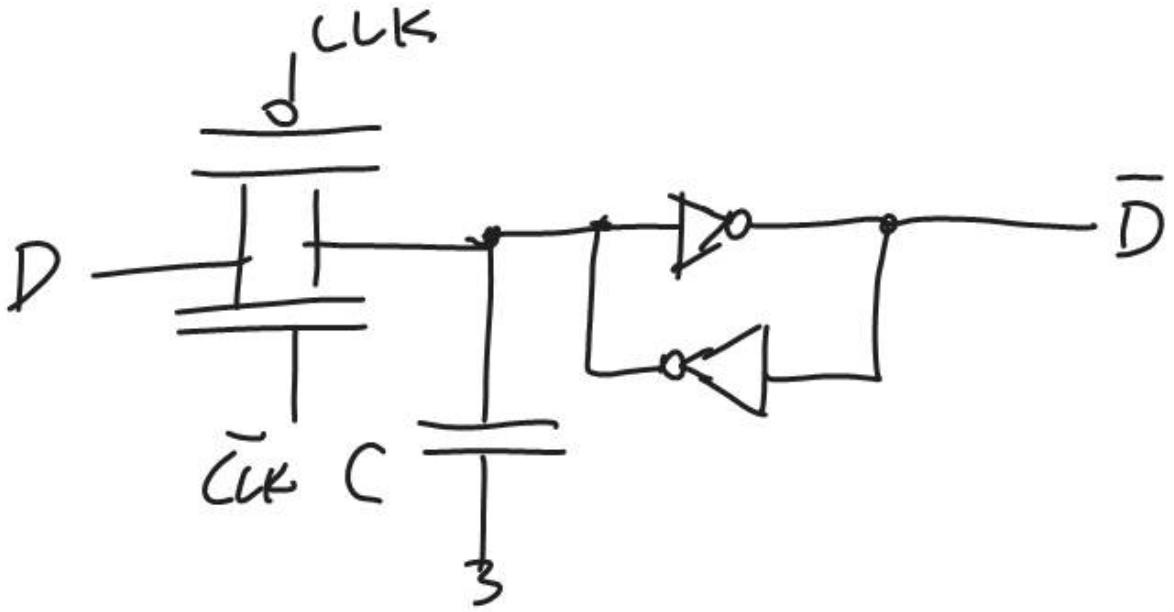
Each C holds 1 bit of information.

DYNAMIC TRANSMISSION GATE EDGE-TRIGGERED REGISTERS



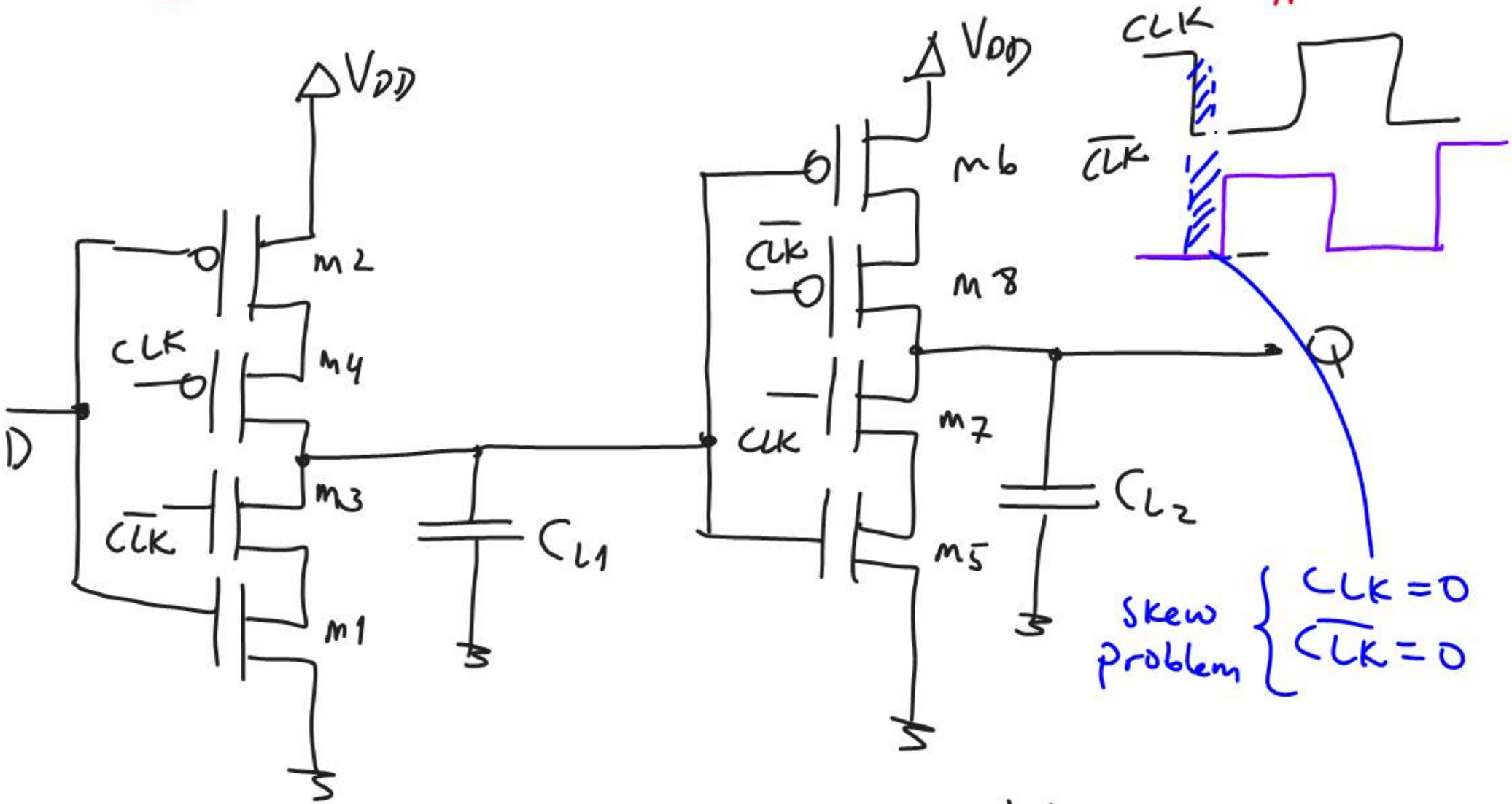
CLK → HIGH ⇒ X is sensed ⇒ $Q = \overline{\overline{X}} = D$

CLK → LOW ⇒ D is sensed ⇒ $X = D$



Pseudo static Latch.

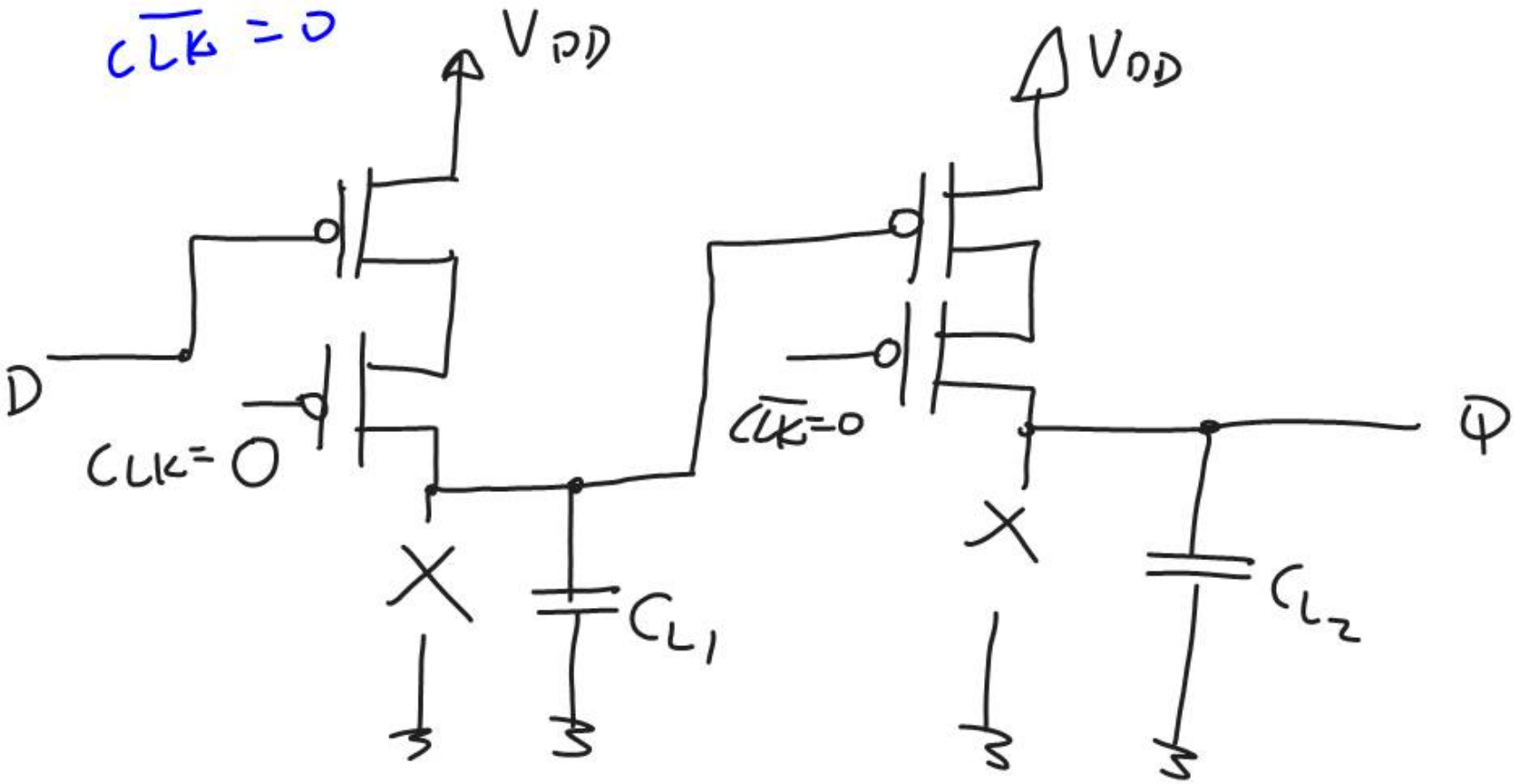
C^2MOS — A Clock Skew insensitive approach



Master-Slave positive edge-triggered register

CLK = 0

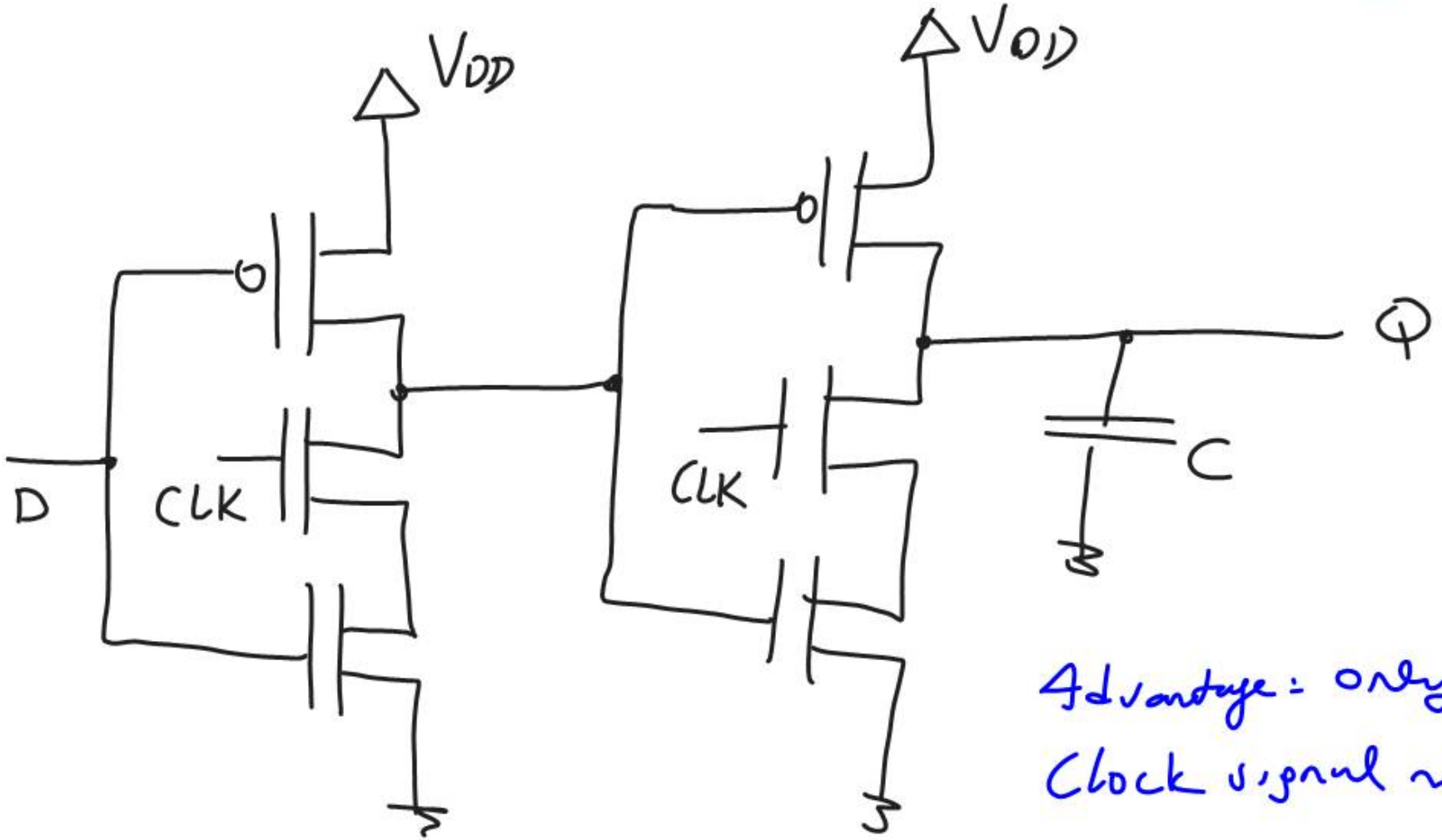
$\overline{CLK}$ = 0



In this case D is not transmitted to output.

∴ This circuit solves the CLK SKEW problem also.

TRUE SINGLE PHASE CLOCKED REGISTERS (TSPCR)

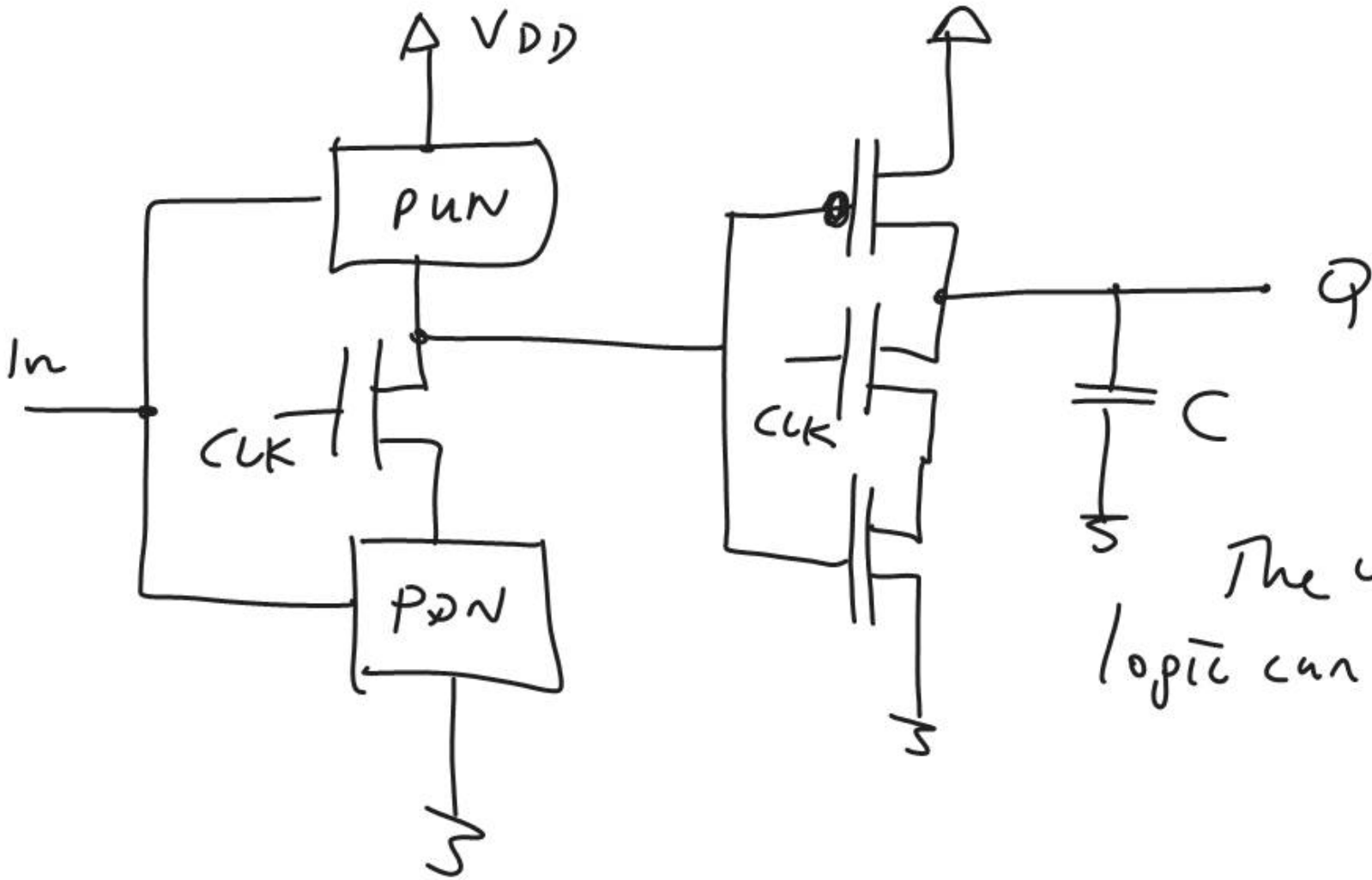


Advantage: only 1 Clock signal needed

This is a LATCH

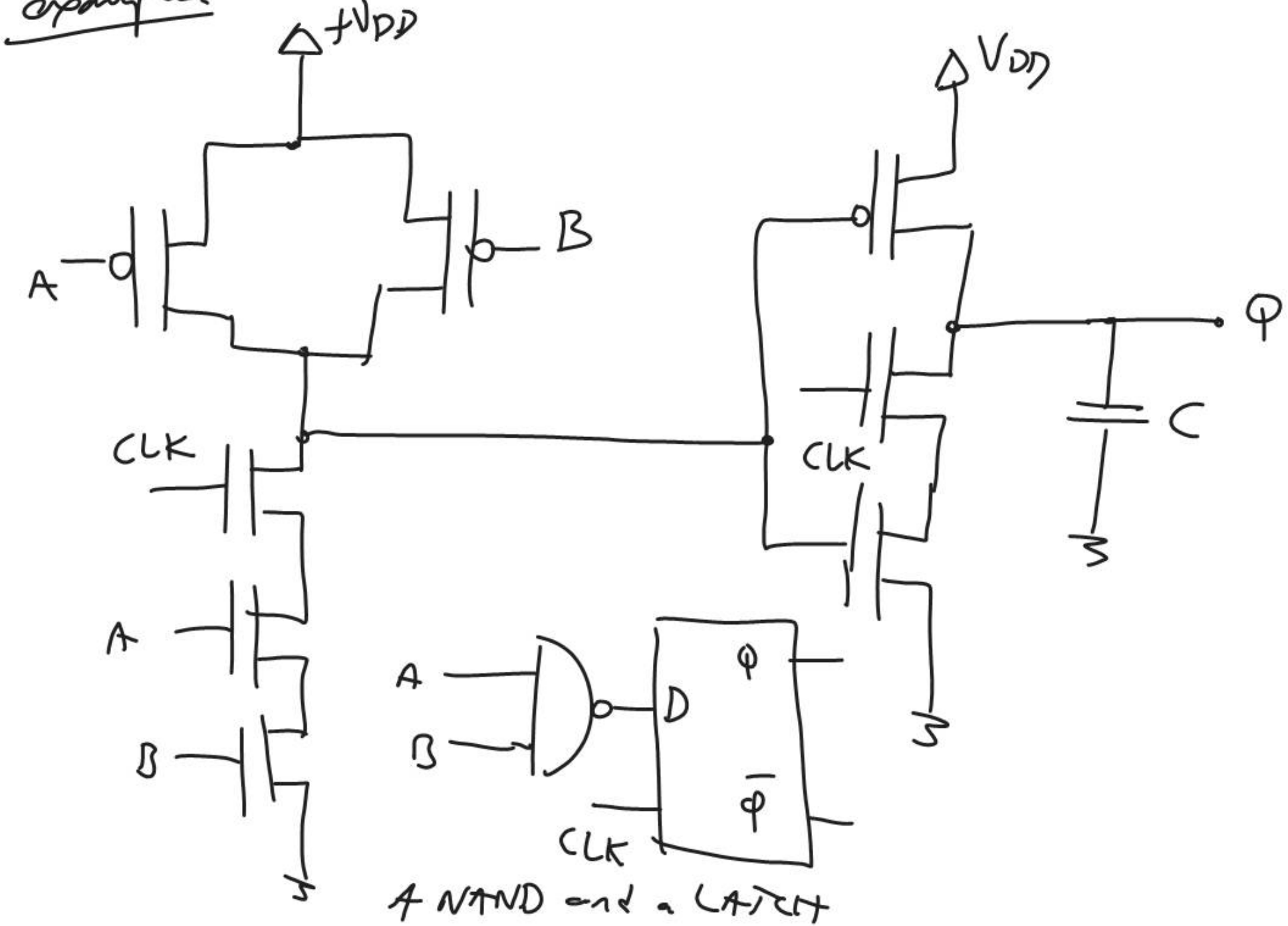
TSPCR offers another advantage:

Other logic functions can be generated at the same time.



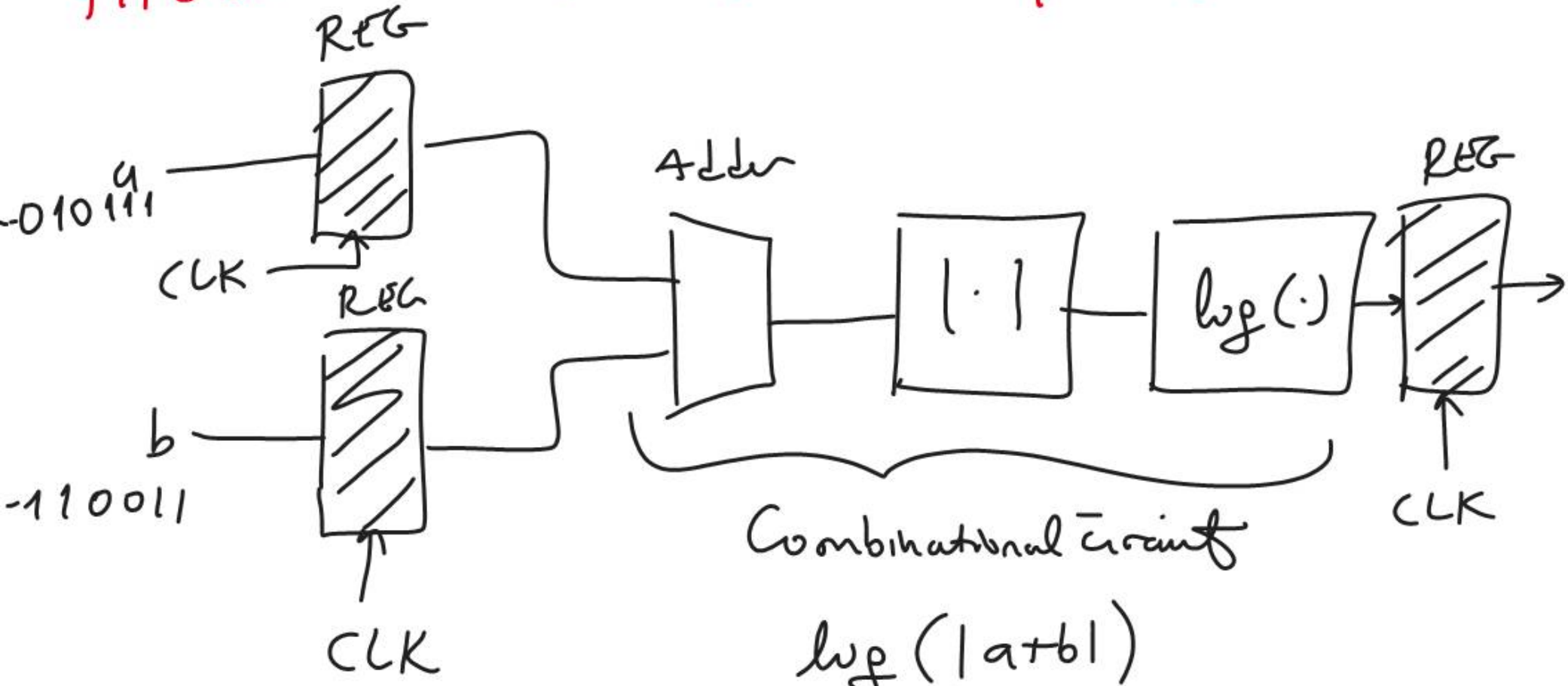
The combinational logic can be implemented too.

example:

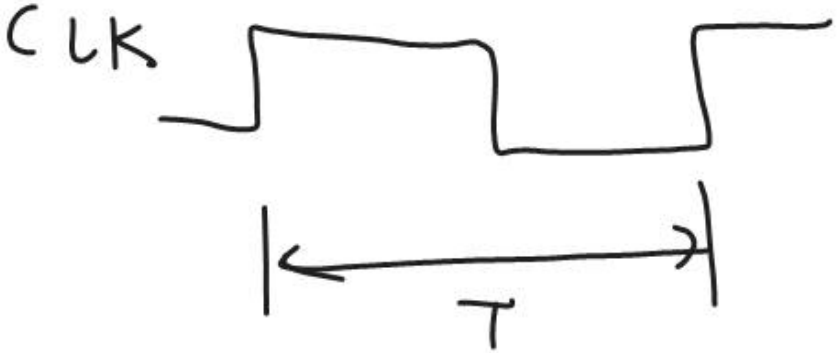


A NAND and a LATCH

PIPELINING → to optimize sequential circuit



$\log(|a+b|)$

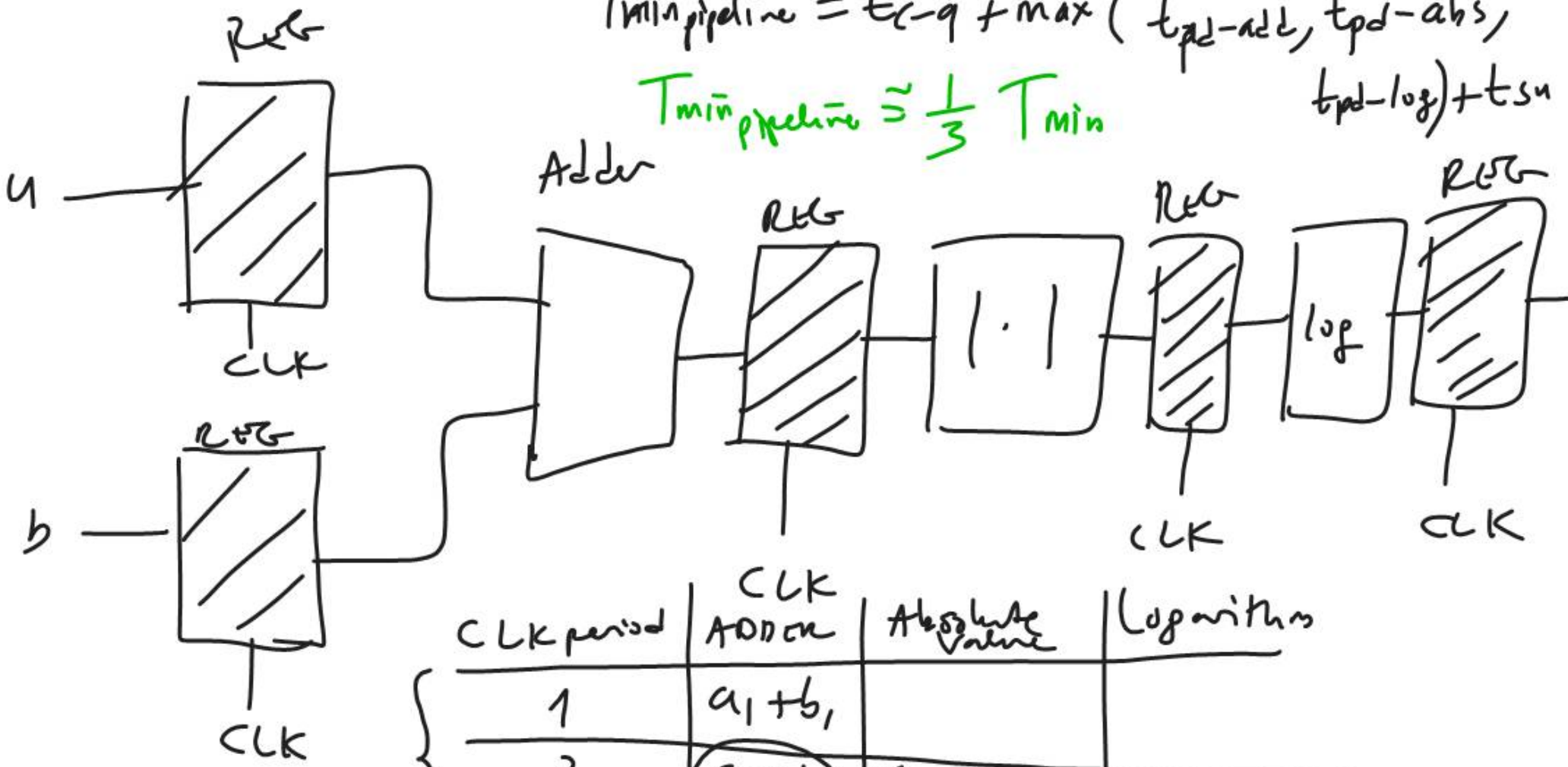


$T_{min} = t_{c-q} + t_{pd-logic} + t_{su}$

A better way:

$$T_{min\,pipeline} = t_{c-q} + \max(t_{pd-add}, t_{pd-abs}, t_{pd-log}) + t_{su}$$

$$T_{min\,pipeline} \cong \frac{1}{3} T_{min}$$



CLK period	CLK Adder	Absolute value	Logarithm
1	a_1+b_1		
2	a_2+b_2	a_1+b_1	
3	a_3+b_3	a_2+b_2	a_1+b_1
4	a_4+b_4	a_3+b_3	a_2+b_2