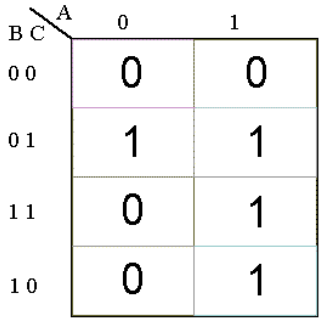
ECE 424 – INTRODUCTION TO VLSI DESIGN + LAB

LABORATORY WORK 4

In this laboratory work, we will design logic circuits by using CMOS logic gates that we had constructed last week.

1) Design a circuit that gives the output f= (A'+B') + (A'.B). While you are designing that circuit, use hierarchy blocks.
2) A Karnaugh map is given in Figure 1. Try to find the output function of that Karnaugh map and construct a logic circuit which has the same characteristic with the map that is given in Figure 1. Don't forget to use hierarchy blocks.



BC \ A	0	1
00	0	0
01	1	1
11	0	1
10	0	1

Figure 1

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