ECE 424
VLSI Design
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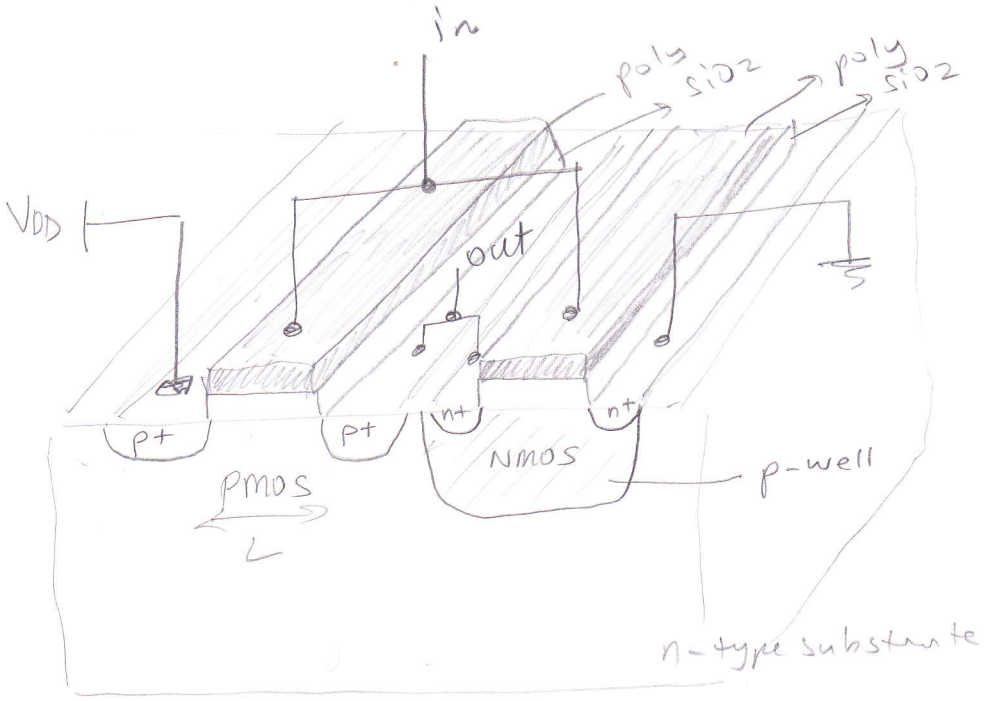
QUESTIONS & EXERCISES

(1) On an n-type Silicon substrate draw and show a CMOS inverter devices and connections. (3-D view)

SOL:



(2) For the drain current (Ids) of an nMOS transistor, determine whether True or false and Explain

a) increases when the channel length (L) increases.

b) decreases when the channel width (W) increases.

c) increases with an increase in Vgs (when it is greater than the threshold voltage V_T)

d) Always increases with the voltage applied between Drain and Source (Vds).

e) There is a parasitic capacitor between gate and the channel and it becomes effective when the signal frequency increases.

(3) Explain why VLSI Design mostly refers to the Digital VLSI Design, but not Analog VLSI Design.

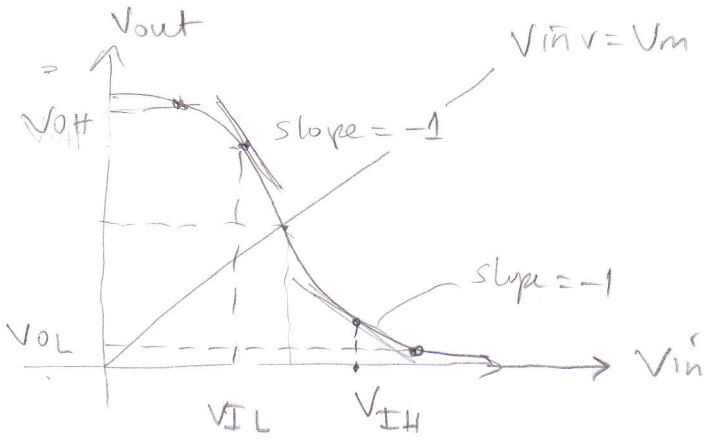
(4) Give an example for each level in the VLSI Digital Design process as given below:

level	Example
1 DEVICE	an MOS transistor
2 CIRCUIT	a CMOS inverter of MOS transistors
3 GATE	a NAND gate from CMOS circuits
4 FUNCTIONAL MODULES	an ADDER from NAND gates
5 SYSTEM	a Processor from Adders, multipliers, registers, etc.

(5) What are the essential Quality metrics for a DIGITAL DESIGN?

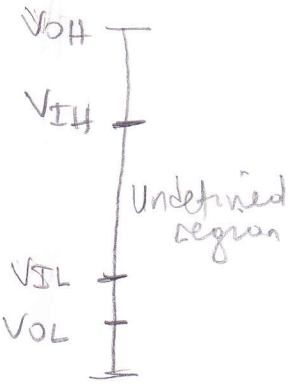
1- cost
2- functionality
3- robustness
4- performance
5- energy consumption

(6) Draw a Voltage Transfer characteristics (VTC) for a CMOS inverter and show on the curve the voltage levels of V_{IH} and V_{IL}. Indicate the inversion voltage V_{inv}.



(7) Explain the difference between the concepts of "NOISE MARGIN" and "NOISE IMMUNITY".

SOL: Noise margin is defined for ex. for a digital circuit as



$NM_H = V_{OH} - V_{IH}$
$NM_L = V_{IL} - V_{OL}$
} This is desired to be as big as possible.

It expresses the capability of the circuit to overpower the noise source.

NOISE IMMUNITY expresses the ability of the system to process and transmit information correctly in the presence of noise, i.e., it expresses the rejection of noise.

(8) Why cooling of the integrated circuits (ICs) at most time is a necessity? Explain.

SOL: The average power consumed by the IC is

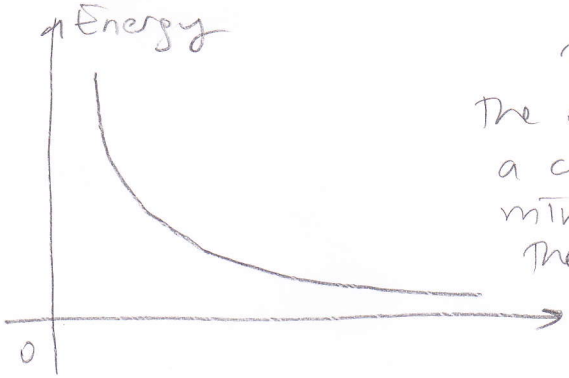
$$P_{ave} = \frac{1}{T}\int_0^T p(t)\,dt = \frac{V_{DD}}{T}\int_0^T i_{supply}(t)\,dt$$

where $p(t)$ is the instantaneous power.

This average power supplied by the power supply is converted into heat by the IC. This heat can get very high due to miniaturisation (hundreds of thousand transistors in mm^2 area of Silicon) and should be dissipated.

We know that $\boxed{\Delta T = \Theta \cdot Q}$ (Heat-flow equation), where ΔT is the change in temperature caused by the heat flow (Q), Θ is the thermal resistance of the package of IC. As heat increases, ΔT increases (i.e. the temperature between the IC and the environment increases) when ΔT becomes higher than a certain limit the IC will burn. In order to keep ΔT in the safe region, the circuit sometimes can not dissipate the amount of the heat generated and must be cooled.

(9)



The objective of a designer of the electronic circuit is to build a circuit which consumes the minimum power while having the fastest time response.

The characteristics shows the general behaviour of an electronic circuit regarding the energy consumed by the circuit and the propagation delay that the circuit introduces. Interpret the characteristics in terms of the power consumption and speed of operation of a circuit.

SOL: The figure shows that when energy is decreased, the delay of the circuit increases and vice versa. That is it shows that $\boxed{\text{Energy} \times \text{Delay} = \text{constant}}$. Therefore there should be always a trade off in the circuit design; when we make it faster, it consumes more power, or if we minimise the power consumption, then the circuit becomes slower.

(10) What semiconducting manufacturing processes are used to dope the semiconductor (i.e. to introduce impurities so that it becomes a p-type or n-type semiconductor)? Explain the principles of the processes.

Sol Diffusion and Ion implantation processes are used to dope the semiconductor.

(Look at the notes for the principles of these processes!)

(11) Why IC packaging with the desired number of pins is becoming a problem as the semiconductor manufacturing technology improves with time? Explain.

Sol: Moore's Law predict that the number of transistors in a chip will double in every 18 month-period.

When the number of devices in an IC chip (die) increases, the inputs/outputs (I/O) requirement of the chip increases with Rent's Rule:

$$P = K \times G^{\beta}$$

where P = the number of I/O pins to the chip (die)

K = average number of I/O per gate

G = the number of gates

β = the Rent exponent (0.1–0.7)

Therefore as G increases P increases too, and to provide desired number of pins in an IC package is becoming a problem.

In 2010 ⇒ we need IC packages of more than 2000 pins!

(12) Thermal resistance of a plastic IC package is given as $\theta = 3.5\ ^\circ C/W$, whereas for a ceramic IC package $\theta = 2.5\ ^\circ C/W$. If the temperature difference between die and environment $\Delta T \leq 75^\circ C$, and the propagation delay for each gate is about $t_p = 2\ nsec$ with the switching energy per gate is $\delta = 0.1\ pJ$, calculate the number of the gates allowed in the chip a) for the plastic package b) for the ceramic package. c) which one dissipates more power?

Sol

$$\frac{N_G}{t_p} \leq \frac{\Delta T}{\theta \cdot \delta} \Rightarrow N_G \leq \frac{\Delta T \cdot t_p}{\theta \cdot \delta}$$

a) for Plastic: $N_G \leq \dfrac{70^\circ C \times 2 \times 10^{-9}\ sec}{3.5^\circ C/W \times 10^{-13}\ J}$

$$N_G \leq \frac{140 \times 10^{4}}{3.5} = 400{,}000\ \text{gates/chip}$$

b) for Ceramic: $N_G \leq \dfrac{70 \times 2 \times 10^{-9}}{2.5 \times 10^{-13}} = \dfrac{140 \times 10^{4}}{2.5} = 560{,}000$ gates/chip

c) $\Delta T = \theta \cdot Q$

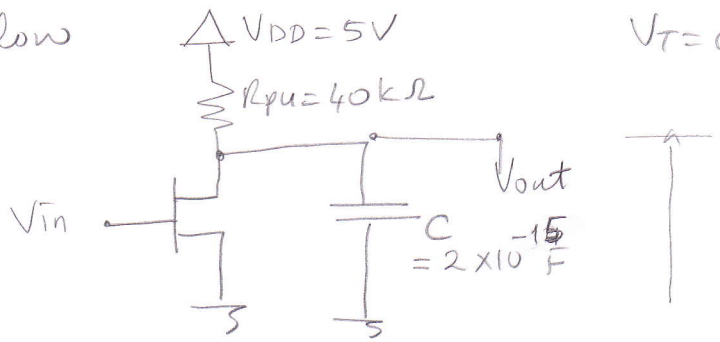
$70 = 3.5 \times Q \quad Q = \frac{70}{3.5}$ for plastic = 28.5 Watts.

$Q = \frac{70}{2.5}$ for ceramic = 56 Watts.

of heat is dissipated

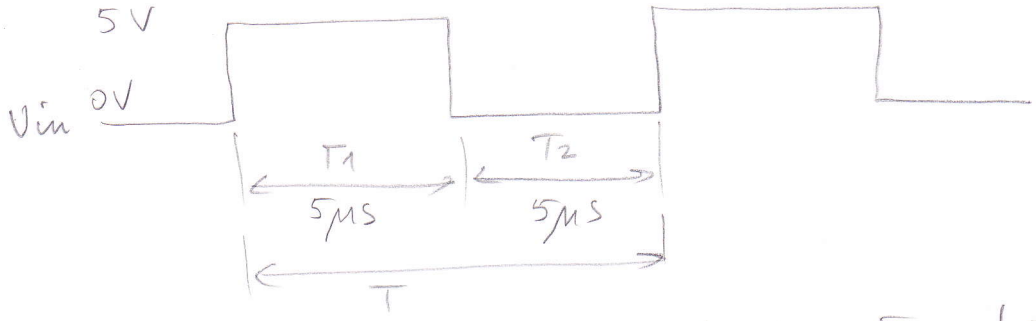
More gates are possible with a ceramic package if lower thermal resistance, since for the same ΔT, ceramic package can dissipate more power than the plastic package.

(13) (Homework Problem) For the basic inverter shown below



$V_T = 0.5\,V$.

and for the input voltage wrt time is given as



a) Calculate the charging and discharging transient times (use $V_{out} = 0.9V_{DD}$ for charging, $V_{out} = 0.2V_{DD}$ for discharging as the limiting values)

b) Calculate the energy consumed during the transients.

c) Where this energy is dissipated? How?

d) Calculate the static power consumed during T.

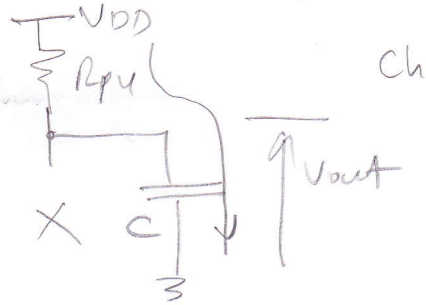
e) What are the disadvantages of this inverter? Explain.

f) Calculate the β of the transistor (Hint: When NMOS is ON)

g) Draw the approximated VTC for the Inverter.

SOL:

a)



Charging when Vin goes from High to Low ⇒ NMOS → Cut off.

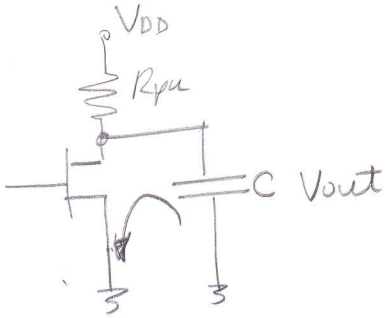
$$V_{out} = V_{DD}\left(1 - e^{-t/RC}\right)$$

$$0.99V_{DD} = V_{DD}\left(1 - e^{-t/RC}\right)$$

$$t_{charging} = 1.84 \times 10^{-10}\ sec. \cong 18\ n\,sec$$

t discharging ⇒ when Vin goes from L to H.

NMOS ⇒ ON



$V_{out} = V_{DD} e^{-t/RC}$

$0.2V_{DD} = V_{DD} e^{-t/RC}$

$t = RC \cdot \ln 0.2$

$t = R_{ch} \cdot C \cdot \ln 0.2$

For $V_{out} = 0.2\,V_{DD}$

$\frac{V_{DD}}{R_{pu}+R_{ch}} \quad R_{ch} = 0.2 V_{DD}$

$R_{ch} = 0.2R_{pu} + 0.2R_{ch}$

$0.8R_{ch} = 0.2R_{pu}$

$\boxed{R_{pu} = 4R_{ch}}$

$R_{ch} = \frac{40k}{4} = 10k$

$t = -10\times10^{3} \times 2\times10^{-12} \ln 0.2$

$t = -20\times10^{-12} \times \ln 0.2$

$t = -2 \ln 0.2 \times 10^{-11}$

$t = 2 \times (1.61) \times 10^{-11}$

$\boxed{t = 3.22 \times 10^{-11}\ s.} \approx 32\ ps$

b) $E_{in} = \int_0^T u(t)\, i(t)\, dt$

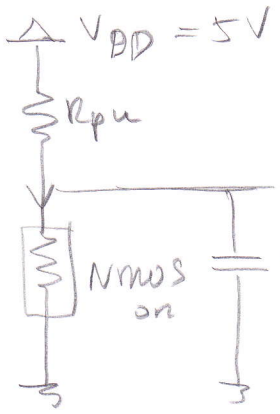
$E_{in} = V_{DD} \int_0^T C \frac{du(t)}{dt} dt = V_{DD} C \int_0^{V_{DD}} du(t) = V_{DD}^2 \cdot C$

$E_{in} = 5^2 \times 2\times10^{-15} = 25 \times 2 \times 10^{-15} = 50\times10^{-15}$ Joules (very small)

c) Half of this energy (i.e. $\frac{CV^2}{2}$) is dissipated on Rpu during charging, and other half is dissipated on the transistor (Rch) during discharging and is converted into heat.

d) Static power consumption:
Transient durations are very small in comparison with the T = 10μs. So we can neglect them.
When the Vin is HIGH → transistor is ON and during this half cycle a static current

from V_{DD} flows to the GND (after transient ends):



$$I_{pu} = \frac{5-1}{40K} = \frac{4}{40K} = 0,1 \times 10^{-3} A.$$

This current flows through the transistor also.

$$I_{pu} = I_{ds}$$

In total we have:

$$P_{ST} = 4V \times 0,1 \times 10^{-3} A + 1V \times 0,1 \times 10^{-3} A = V_{DD} \times I_{ds}$$

$$= V_{DD} \times 0,1 \times 10^{-3} A = 5 \times 0,1 \times 10^{-3} = 0,5 \times 10^{-3} \text{ Watts.}$$

when $V_{in} = 0$ (Low) (CUT OFF). A very short-time transient current will flow. When the capacitore charges to V_{DD} voltage, no current will flow through the Rpu. Therefore, except transient there will be no static power dissipated in this half cycle. Hence, the static power is consumed only for the cycle when the NMOS transistor is ON.

$$\boxed{P_{ST} = 0,5 \times 10^{-3} \text{ Watts.}}$$ ← NMOS transistor is ON.

e) → charging and discharging times are not symmetric this comes a distortion in the output signal

→ Due to Rpu, a static current will flow when $V_{in} \Rightarrow$ HIGH. This comes a static power to be dissipated at this half cycle. Big static power dissipation is another disadvantage of this type of inverter (Basic inverter circuit).

f) When NMOS is ON, the $V_{out} = 0,2 V_{DD} = 1V = V_{ds}$

$V_{gs} = V_{in} = 5V. \Rightarrow \boxed{V_{gs} - V_T > V_{ds}} \Rightarrow 5 - 0,5 > 1$

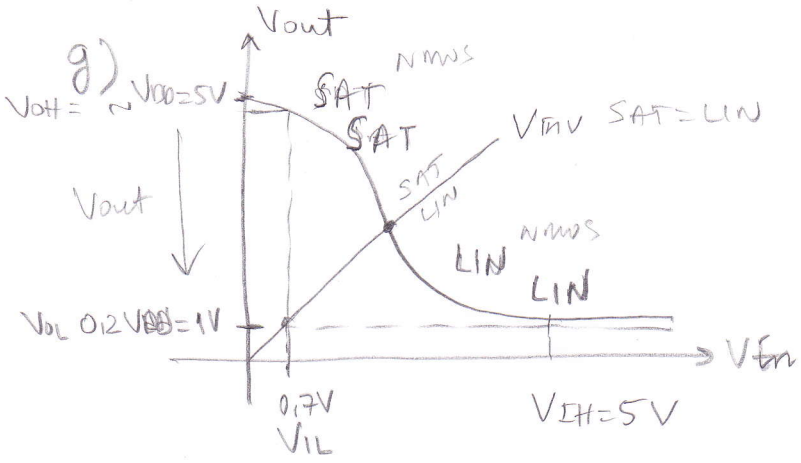
the transistor is in the linear region!

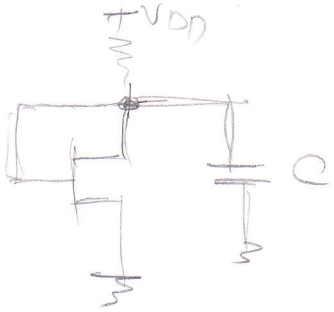
$$I_{ds} = \beta \left(V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds}$$

$$\boxed{I_{ds} = I_{pu} = 0,1 \times 10^{-3} A}$$ when NMOS is ON.

$$0,1 \times 10^{-3} = \beta \left(5 - 0,5 - \frac{1}{2} \right) 1 \Rightarrow \beta = \frac{0,1 \times 10^{-3}}{4} = 0,025 \times 10^{-3} \frac{A}{V^2}$$

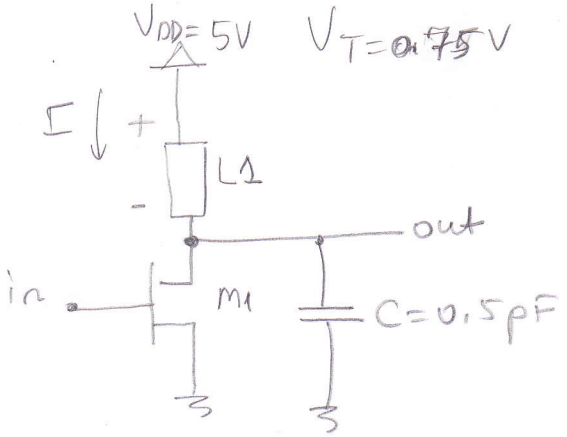
g)

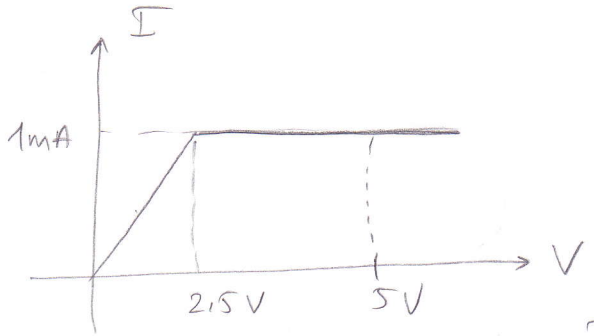




When $V_{in} = V_{out}$

(14) Consider the fictitious gate as shown in the Figure The I-V characteristics of the load device L1 is given





$\mu = 1350\ cm^2/V\text{-}s$
$\epsilon = 11.8 \times 8.85 \times 10^{-14}\ F/cm$
$t_{ox} = 1000\ A^\circ$
$V_T = 0.75V$

a) Determine $(W/L)_{M1}$ such that a V_{OL} of 1V is obtained.

b) Write down the equation(s) you would use to solve for V_{IH}.

c) find t_{pHL}

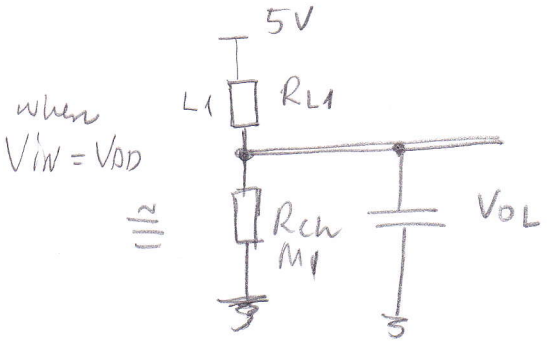
d) Determine the average static power consumption assuming that the input is high 70% of the time.

e) Determine how much energy is dissipated as heat for one clock cycle. (T = 1 μsec)

SOL: in the following pages:

a) $V_{OL} = V_{out_L} = 5V \cdot \frac{R_{ch}}{R_L + R_{ch}} = 1V$

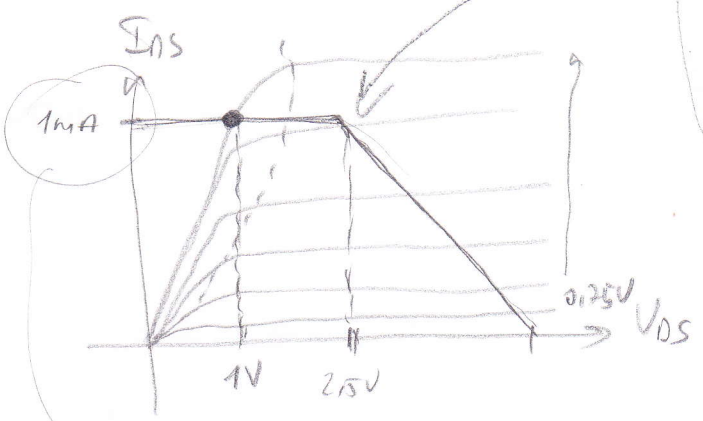
$\frac{R_{ch}}{R_L + R_{ch}} = \frac{1}{5}$ $\quad 5R_{ch} - R_{ch} = R_L$ $\quad 4R_{ch} = R_L$ $\quad \frac{R_{ch}}{R_L} = \frac{1}{4}$



When $V_{OL} = 1V$, then across the device $L_1 = 5 - 1 = 4V$.

$R_{L_1} = \frac{4V}{1mA} = 4k\Omega.$

$R_{ch} = \frac{1}{4} \times R_L = \frac{1}{4} \times 4k = 1k\Omega.$



M_1 operates in the linear region ($V_{DS} = 1V$ across M_1)

$I_{ds} = \beta \left(V_{gs} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$ (Linear Region)

$V_{out} = V_{DS} = 1V$ for M_1

$V_{GS} = 5V$

$\beta \left(V_{gs} - V_T - \frac{V_{DS}}{2} \right) V_{DS} = 1mA$

$\beta = \frac{10^{-3}}{(V_{gs} - 0.7V - 0.5) \cdot 1}$

$\beta = \frac{10^{-3}}{4.3 - 0.5} = \frac{10^{-3}}{3.8}$

$\beta = \left(\frac{\mu \epsilon}{t_{ox}} \right) \frac{W}{L} = \frac{10^{-3}}{3.8} = 0.26 \times 10^{-3}$

$\frac{\mu \epsilon}{t_{ox}} = \frac{1350 \times 11.8 \times 8.85 \times 10^{-14}}{1000 \times 10^{-8}} = 1.41 \times 10^{-4} \frac{1}{\Omega}$

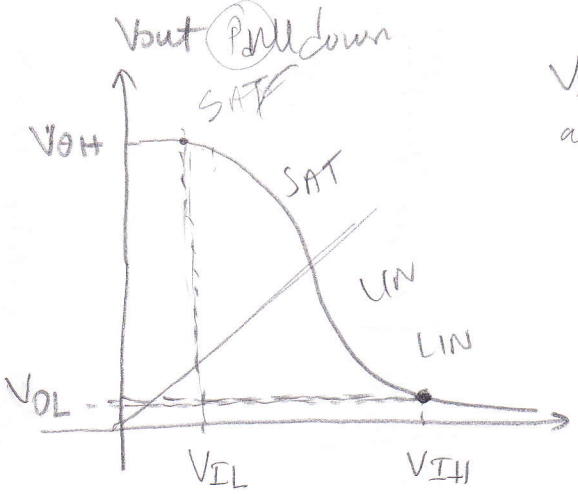
$\frac{W}{L} = \frac{0.26 \times 10^{-3} \left(\frac{1}{\Omega}\right)}{1.41 \times 10^{-4} \left(\frac{1}{\Omega}\right)}$

$\frac{cm^2/Vs \cdot F/cm}{cm} = \frac{F}{Vs} = \frac{1}{\Omega}$

$\frac{W}{L} = 1.84$

For $\mu = 1350 \, cm^2/V\text{-}s$,
$\epsilon = 11.8 \times 8.85 \times 10^{-14} \, F/cm$
$t_{ox} = 1000 A^\circ$
$V_T = 0.7V$

b)



V_{IH} is the input voltage that creates V_{OL} at the output.

① $I_{ds} = \beta \left(V_{IH} - V_T - \frac{V_{OUT_L}}{2} \right) V_{OUT_L}$

② $I_{ds} = 1\,mA$ and $V_{OUT_L} = 1V$

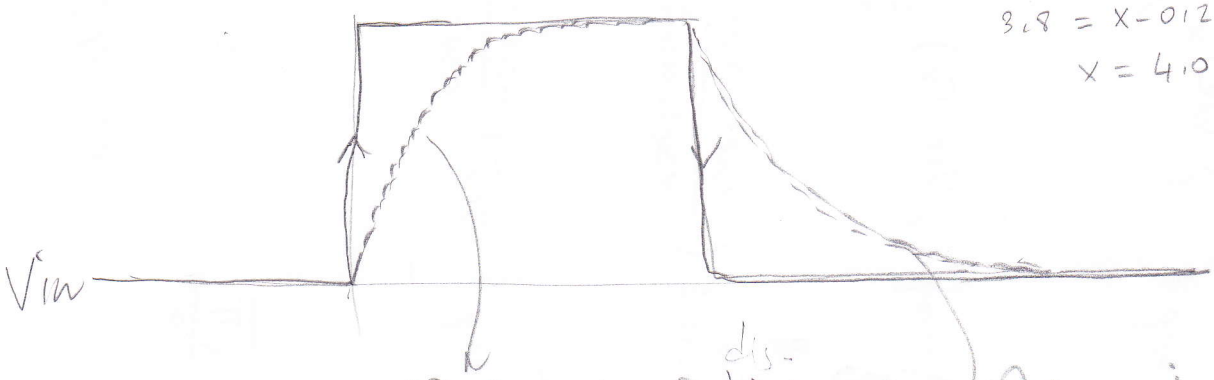
From these equations V_{IH} is calculated.:

$$10^{-3} = \left(\frac{10^{-3}}{3.8}\right)(x - 0.7 - 0.5)\,1$$

$$3.8 = x - 0.2$$

$$x = 4.0 \rightarrow \boxed{V_{IH} = 4V}$$

c) $t_{pHL} = ?$

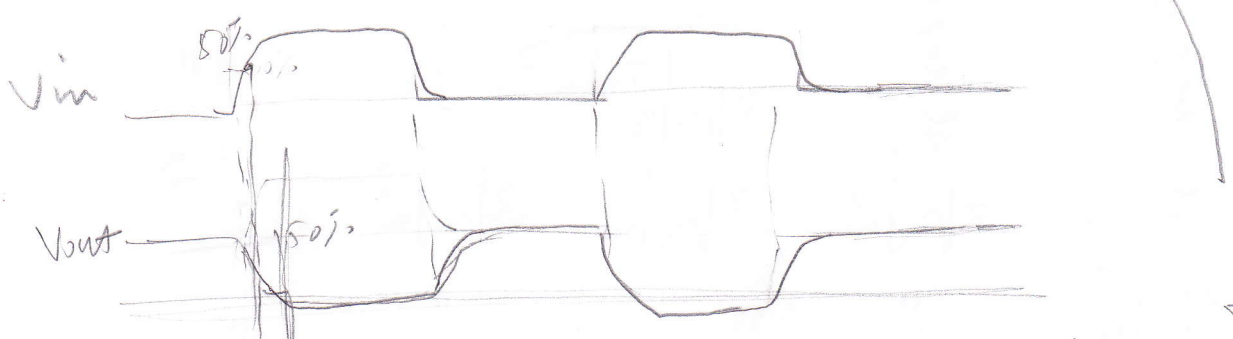


① Capacitor is discharging Through M_1

$V_{OUT} = V_{in}\, e^{-t/RC}$

② Capacitor is Charging Through L_1

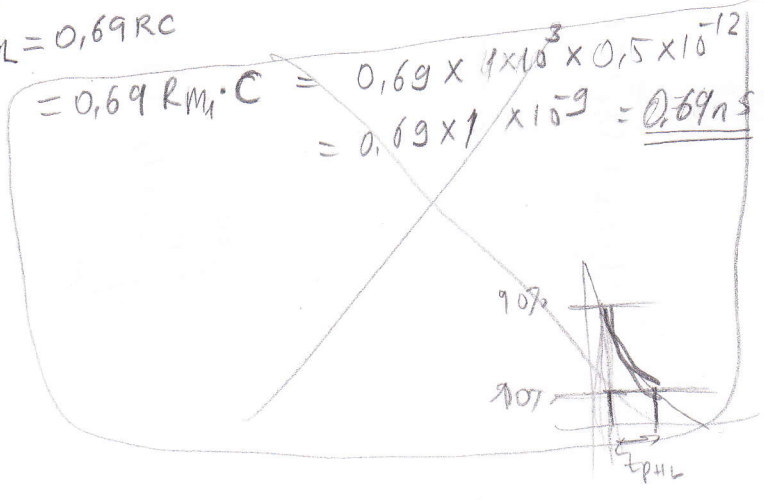
$V_{OUT} = V_{IN}(1 - e^{-t/RC})$



$t_{pHL} = 0.69RC$

$= 0.69\, R_{M_1} \cdot C = 0.69 \times 1\times10^{3} \times 0.5 \times 10^{-12}$

$= 0.69 \times 1 \times 10^{-9} = \underline{0.69ns}$



$0.2V_{DD} = V_{DD}\, e^{-t/RC}$

$-t = R_{ch} C \ln 0.2$

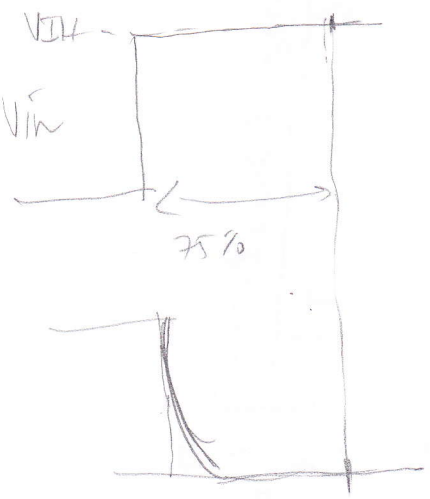
$-t = 10^{3} \times 0.5 \times 10^{-12} \times (-1.61)$

$t = \underline{0.3 \times 10^{-9}\,sec = 0.9nsec}$

$t_{pHL} = 0.3 \times 0.9 = 2.7nsec$

1) When input is high for 75% of time:

① Capacitor is discharging for a very short time through M_1 and then



$I_{ds} = 1mA$ constantly flowing through M_1 and L_1 at $V_{out} = 1V$.

When $V_{out} = 1V$

V_{DS} for $L_1 = 5 - 1 = 4V$

V_{DS} for $M_1 = 1V$.

$P_{av_{L_1}} = 4 \times 10^{-3} = 4mW$

$P_{av_{M_1}} = 1 \times 10^{-3} = 1mW$

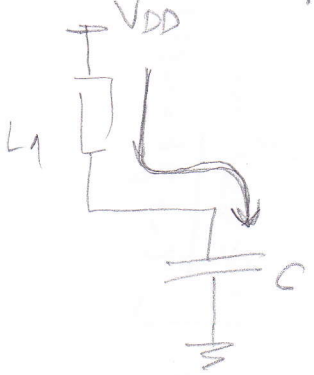
Totally = 5mW is dissipated statically for 75% of time.

However, for 25% of clock time $V_{in} \Rightarrow$ Low.

This drives M_1 to cut off.

Capacitor charges through L_1 for a transient time, except for this the static power consumption is:

$$P_{av} = \frac{1}{0,25T}\int_0^{0,25T} p(t)\,dt = \frac{V_{DD}}{0,25T}\int_0^{0,25T} i_{supply}(t)\,dt$$



$i_{supply}(t) \simeq 0$ (we assume) very small!

$P_{av} = 0$

or

$$P = V_{DD}\int_0^{T/2} C\frac{dv_d}{dt}dt = V_{DD}\int_0^{V_{DD}} dv_d\,C = CV_{DD}^2$$

Therefore, in total we have ⇒ for 75% time 5mW of static power consumption,

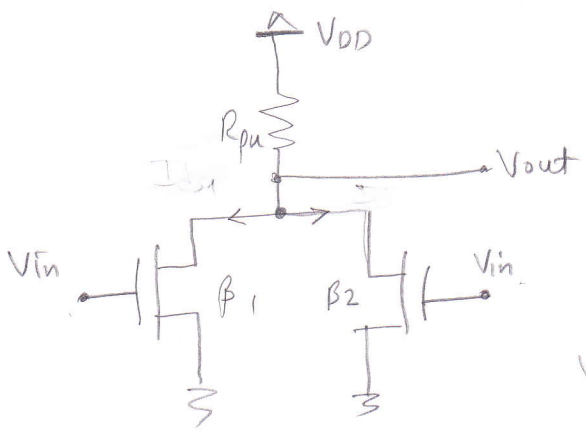
Energy Consumption in a cycle $= 0,75 \times 10^{-6}\,sec \times 5mW = 3,75\mu Joule$ for a clock period energy consumption of the circuit.

(15) (Mukherjee Chap 2 exercise 2.1)

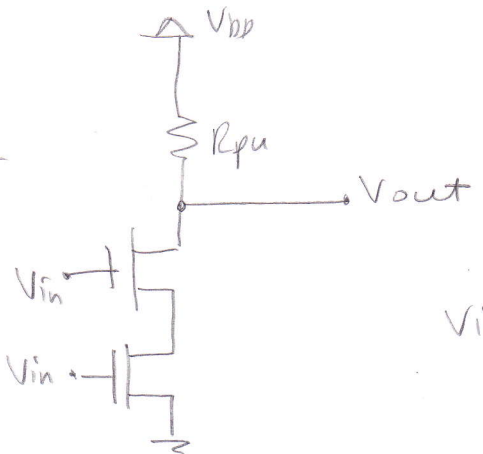
A NOR and a NAND gate is shown below. Assume that β_1 and β_2 denote the quantity β for the two transistors in the pull-down network.

a) Write equations describing the linear and saturated currents flowing in the pull-down circuit when both the transistors are connected to the same input voltage Vin.

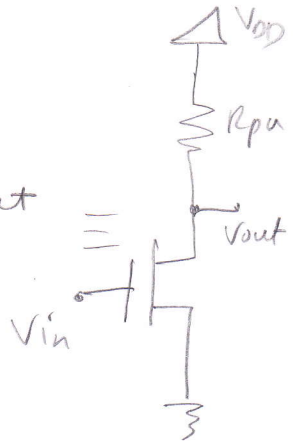
b) From these equations determine the equivalent β, (β_{NOR}, β_{NAND}) for the NOR and the NAND gates, respectively, for the single pull-down transistor which can replace the pull-down circuit.



NOR Gate



NAND Gate



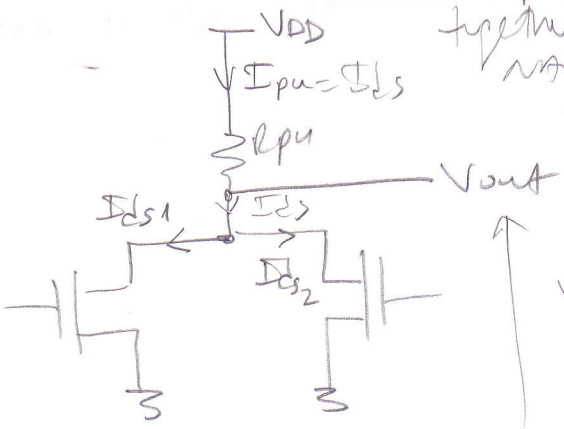
(when both inputs are connected together NOR and NAND gates become inverter)

SOL: a) For the NOR gate:

$$I_{ds} = I_{ds1} + I_{ds2}$$

$$I_{ds} = I_{pu} = \frac{V_{DD} - V_{out}}{R_{pu}}$$

$I = I_{ds1} + I_{ds2}$, and



$V_{ds} = V_{out}$ for both transistors since they are in parallel configuration.

$$I = \beta_1 \left(V_{gs} - V_{th} - \frac{V_{out}}{2}\right) V_{out} + \beta_2 \left(V_{gs} - V_{th} - \frac{V_{out}}{2}\right) V_{out}$$

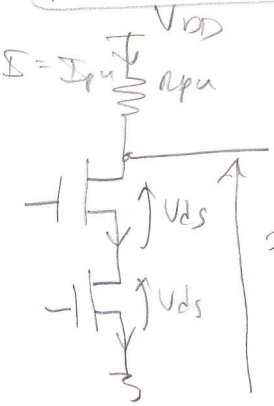
$$\boxed{I = (\beta_1 + \beta_2)\left(V_{gs} - V_{th} - \frac{V_{out}}{2}\right) V_{out}}$$ in the linear region for the NOR gate ($V_{gs} - V_{th} > V_{ds}$)

$$\boxed{I = \left(\frac{\beta_1 + \beta_2}{2}\right)(V_{gs} - V_{th})^2}$$ in the saturation region $0 \le V_{gs} - V_{th} \le V_{ds}$

$$\boxed{(\beta_1 + \beta_2) = \frac{I}{\left(V_{gs} - V_{th} - \frac{V_{out}}{2}\right) V_{out}}}$$ linear

$$\boxed{\beta_1 + \beta_2 = \frac{2I}{(V_{gs} - V_{th})^2}}$$ for SAT

For the NAND gate:



Same current flows through each transistors (since they are in series configuration)

$$I_{pu} = I = I_{ds_1} = I_{ds_2}$$

, whereas $V_{ds} = \frac{V_{out}}{2}$ for each transistor. (Voltage is divided since they are in series connection)

$$2V_{ds} = V_{out}$$

$$V_{ds} = \frac{V_{out}}{2}$$

$$\boxed{\beta_{1_{SAT}} = \beta_{2_{SAT}} = \frac{2I}{(V_{gs} - V_{th})^2}}$$ SAT

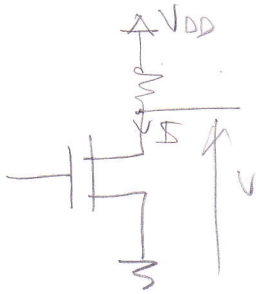
$$I = I_{ds_1} = I_{ds_2} = \frac{\beta_1}{2}(V_{gs} - V_{th})^2 = \frac{\beta_2}{2}(V_{gs} - V_{th})^2$$ for SAT. region

$$I = \beta_1 \left(V_{gs} - V_{th} - \frac{V_{out}}{4}\right) \frac{V_{out}}{2} = \frac{\beta_1}{2}\left(V_{gs} - V_{th} - \frac{V_{out}}{4}\right) V_{out}$$

$$= \frac{\beta_2}{2}\left(V_{gs} - V_{th} - \frac{V_{out}}{4}\right) V_{out}$$ for the linear region

$$\boxed{\beta_{1_{LIN}} = \frac{2I}{\left(V_{gs} - V_{th} - \frac{V_{out}}{4}\right) V_{out}} = \beta_2}$$

b)) For an equivalent 1 transistor for the pull-down: (NAND, and NOR becomes inverter gate in this case though!)



$$I_{ds} = I_{pu} = I = \frac{\beta}{2}(V_{gs} - V_{th})^2$$ for SAT

$$\boxed{\beta_{SAT} = \frac{2I}{(V_{gs} - V_{th})^2}}$$ for SAT

$$I_{ds} = I_{pu} = I = \beta\left(V_{gs} - V_{th} - \frac{V_{out}}{2}\right) V_{out}$$ for LIN

$$\boxed{\beta_{LIN} = \frac{I}{\left(V_{gs} - V_{th} - \frac{V_{out}}{2}\right) V_{out}}}$$

For SAT REGION

$\beta = (\beta_1 + \beta_2) \Rightarrow \underbrace{\beta_1 = \beta_2}_{\text{NAND}}$

β → one pull-up transistor

NOR

For LINEAR REGION

$\beta = (\beta_1 + \beta_2) \Rightarrow \cong \underbrace{\frac{\beta_1}{2} = \frac{\beta_2}{2}}_{\text{for NAND}}$

NOR

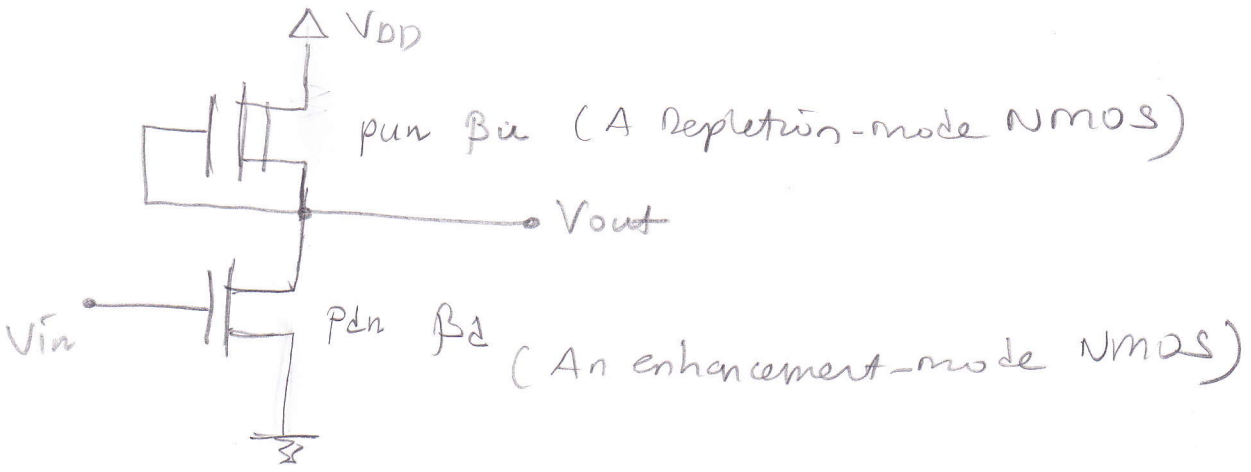
As a result:

In NOR gate pull-down transistors may have $\left(\frac{\beta}{2}\right)$ of the transistor when used in single in the pull-down

In NAND gate however, the pull down transistors have (2β) of the transistor when used in single in the pull down.

(16) a) Will the circuit given below solve the static power dissipation problem? Explain

b) Show how the β's of the transistors (β_{pd}, β_{pu}) are important in determining the V_{LO} voltage.



SOL. a) This circuit solves the asymmetry problem during charging and discharging but does not solve the static power dissipation problem. When Vin is HIGH, pdn NMOS transistor turns ON, since pun NMOS is always ON,

In this case a static current will flow from VDD to GND, through the both transistors. The power (static) dissipated then

$$P_{ST} = I_{ds} \times V_{DD}$$

during this cycle.

b) When Vout becomes low $\rightarrow V_{OL} \cong 0.12\, V_{DD} = V_{out}$

pdn transistor is in Linear region (since the output voltage $V_{OL} = V_{ds}$ of pull down. Since $V_{gs} \cong V_{DD}$ to drive the pdn NMOS transistor

$V_{gs} - V_{th} > V_{ds} \Rightarrow$ Linear Region for pull down with $V_{out} = V_{OL}$.

However, since $V_{ds} = V_{DD} - V_{out}$ for the pull-up depletion mode NMOS, its V_{ds} becomes $\approx V_{DD}$ and it is in SATURATION. Since in both of them, the same Ids will flow:

$$I_{ds} = \beta_d \left(V_{gs} - V_{th} - \frac{V_{OL}}{2}\right) V_{OL} = \frac{\beta_u}{2} (V_{dep})^2$$

pull-down in LINEAR — Pull-up in SAT

$$\beta_d (V_{gs} - V_{th}) V_{OL} \cong \frac{\beta_u}{2} (V_{dep})^2$$

we neglect $\frac{V_{OL}}{2}$ since V_{OL} is small.

$$V_{OL} \cong \frac{\beta_u}{2\beta_d} \frac{(V_{dep})^2}{V_{gs} - V_{th}}$$

$V_{gs} - V_{th} \cong V_{DD}$

$$V_{OL} \cong \frac{1}{2k} \frac{(V_{dep})^2}{V_{DD}}$$

$k = \frac{\beta_d}{\beta_u}$ (Ratio of inverter)

$k = \frac{(W/L)_d}{(W/L)_u}$

Therefore, in satisfying the V_{LO} small, β_d and β_u are important.

(17) Explain why the transient times (charging and discharging) are symmetric and There is no static power consumption in a CMOS Inverter.

SOL: From your notes.

---

(18) Realize $F = AB + BC$ a) with NMOS transistors b) with CMOS circuits

SOL

a) $\bar{F} = \overline{AB+BC} = (\overline{AB}) \cdot (\overline{BC}) = (\bar{A}+\bar{B}) \cdot (\bar{B}+\bar{C})$

$\bar{F} = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{B} + \bar{B}\bar{C}$

$\bar{F} = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B} + \bar{B}\bar{C}$

$\bar{F} = \bar{A}\bar{B} + \bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$

$\bar{F} = \bar{B}(\bar{A}+1) + \bar{A}\bar{C} + \bar{B}\bar{C}$

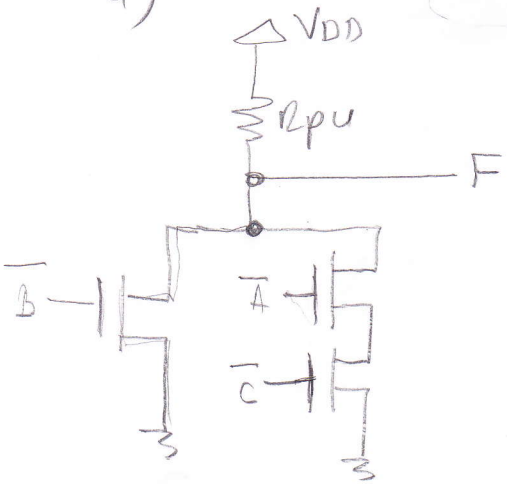
$\bar{F} = \bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$

$\bar{F} = \bar{B}(1+\bar{C}) + \bar{A}\bar{C}$

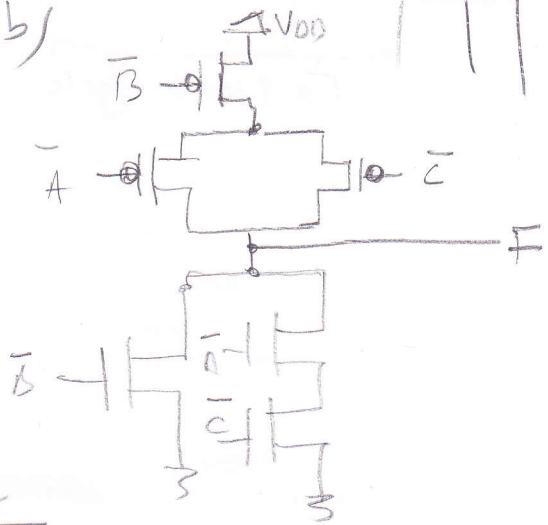
$\boxed{\bar{F} = \bar{B} + \bar{A}\bar{C}}$ ✓

A B C	AB	BC	F	$\bar{F}$	$\bar{B}\bar{C}$	$\bar{B}$
0 0 0	0	0	0	1	1	1
0 0 1	0	0	0	1	0	1
0 1 0	0	0	0	1	1	0
0 1 1	0	1	1	0	0	0
1 0 0	0	0	0	1	0	1
1 0 1	0	0	0	1	0	1
1 1 0	1	0	1	0	0	0
1 1 1	1	1	1	0	0	0

a)



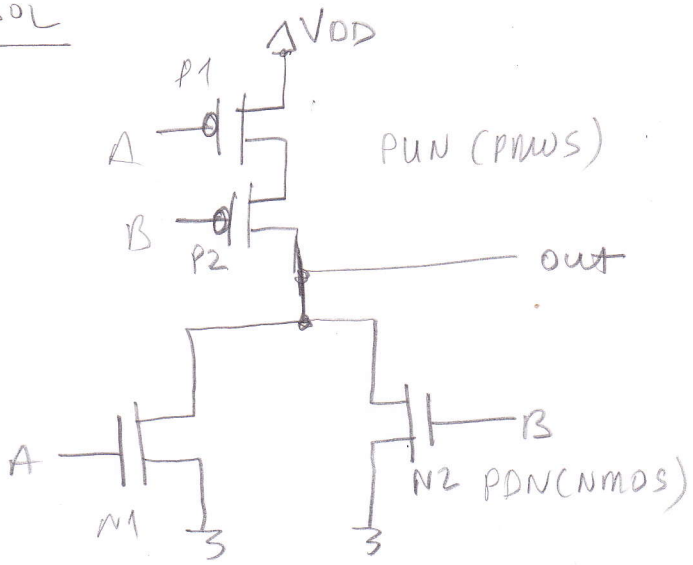
b)

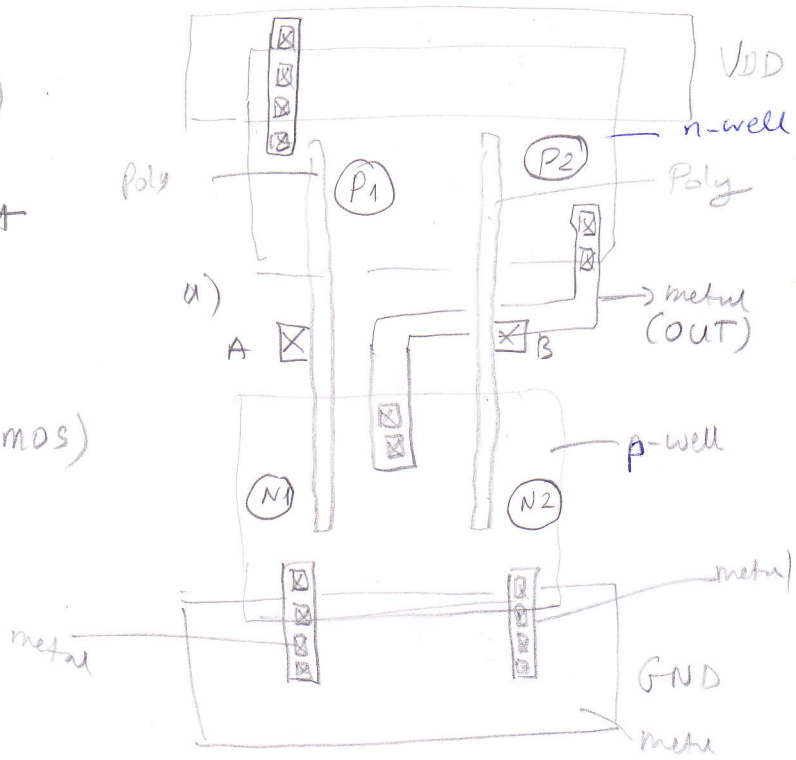


(X) → the complement of F is realized by the PDN

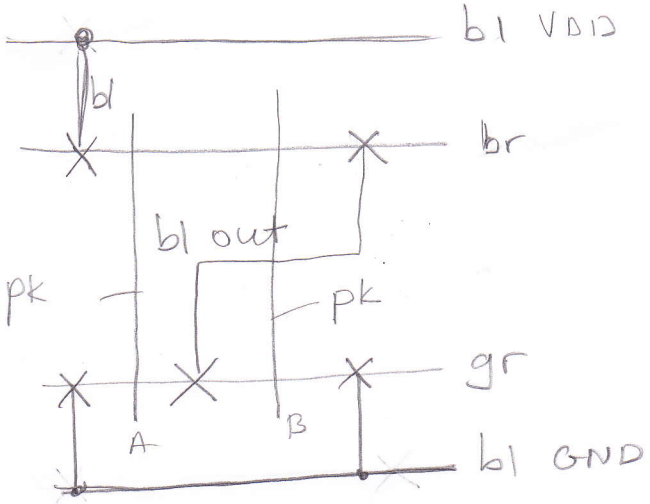
(19) a) Draw the silicon layout for a NOR gate (CMOS)
b) Draw the stick diagram for the same circuit

SOL





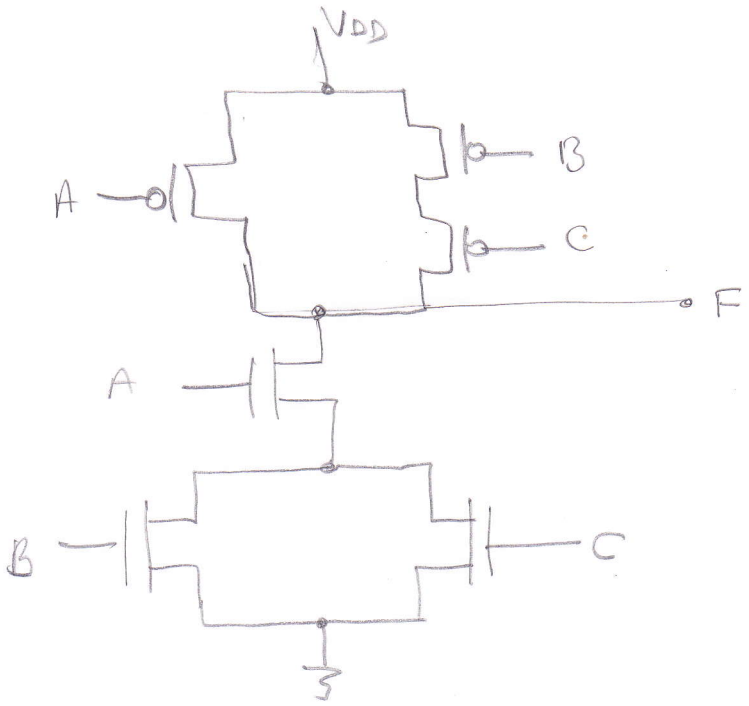
b)



bl = blue = metal
br = brown = p-active
gr = green = n-active
pk = pink = poly

(21) Implement the function $F = \overline{A} + \overline{B}\,\overline{C}$ with CMOS circuits.

SOL $\overline{F} = \overline{\overline{A} + \overline{B}\,\overline{C}} = A \cdot (B + C)$



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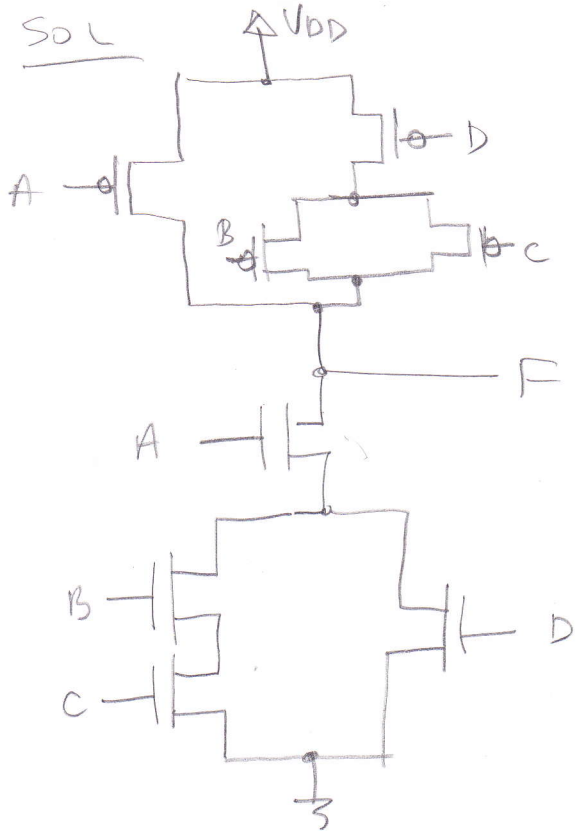
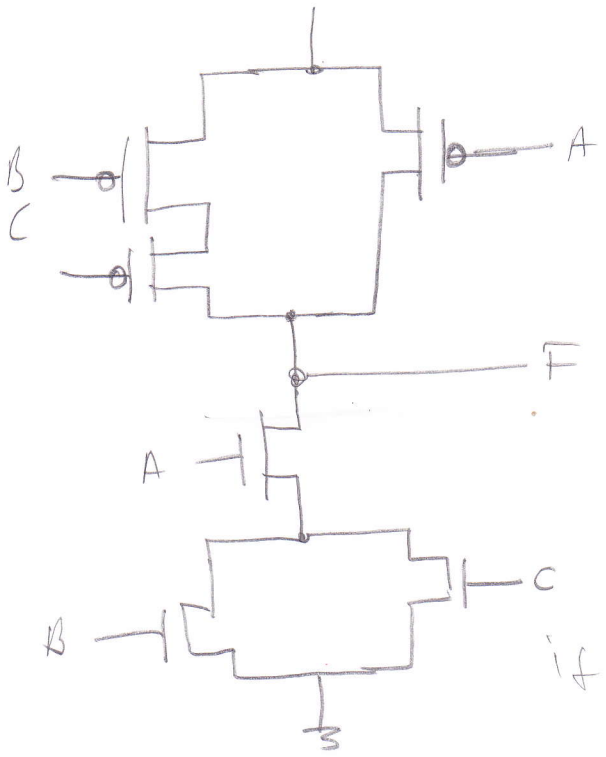
(22) Realise the function $F = \overline{A} + (\overline{B} + \overline{C})\overline{D}$ with CMOS.

$$\overline{F} = A \cdot \left[\overline{(\overline{B} + \overline{C}) + \overline{D}}\right] = A\,[BC + D] = ABC + AD$$

SOL



(23) Derive the function $\bar{F}$ for the CMOS circuit



Sol: Starting from the PDN:

$$F = \overline{A \cdot (B+C)}$$

$$F = \bar{A} + (\bar{B}\bar{C})$$

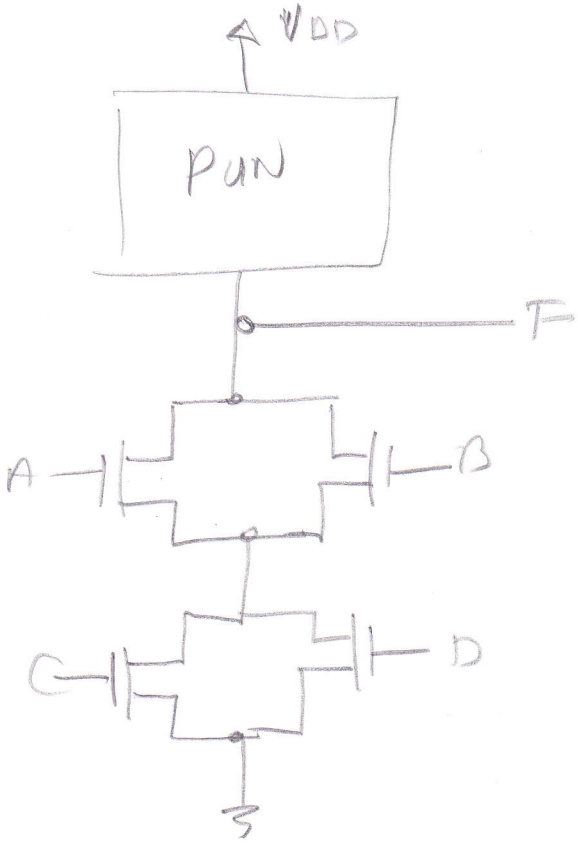
$$\boxed{F = \bar{A} + \bar{B}\bar{C}}$$

---

if $\bar{F} = A \cdot (B+C) \Rightarrow F = \bar{\bar{F}}$

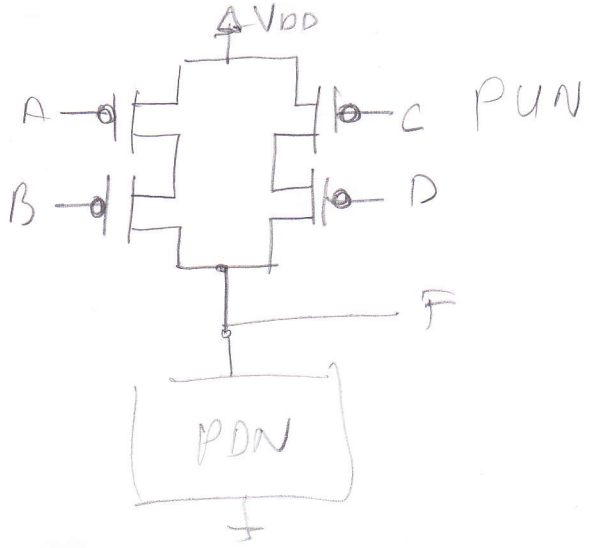
$$F = \overline{A(B+C)} = \bar{A} + (\bar{B}\bar{C})$$

(24) For the PDN given below, obtain the PUN and the function F.

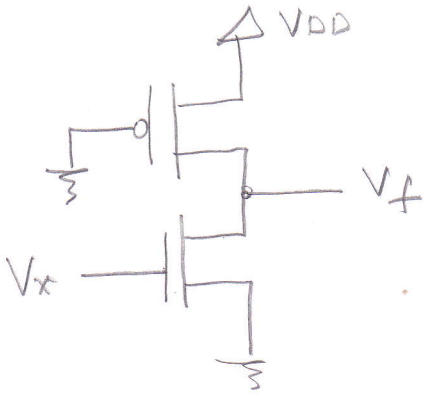


Sol:

$$F = \overline{(A+B)(C+D)}$$



(25) The circuit for the INVERTER given below is called as PSEUDO-NMOS circuit. The Pull-up device (PMOS transistor) is called a "weak" PMOS transistor because it has a small W/L ratio.



When $V_x = V_{DD}$, V_f has a low value. The NMOS transistor is operating in the LINEAR region, while the PMOS limits the current flow because it is operating in the SATURATION region. The current through the NMOS and PMOS has to be equal. Show that the low-output voltage V_{OL} is given by

$$V_{OL} = (V_{DD} - V_T)\left[1 - \sqrt{1 - \frac{\beta_{pu}}{\beta_{pd}}}\right]$$

Sol: When Vx is HIGH = VDD, the output goes low i.e. $V_{ds} = V_{OL}$ and and NMOS is in LINEAR, while PMOS's $V_{ds} = V_{DD} - V_{OL} \Rightarrow$ and PMOS operates in the SAT region. Since the current through the transistors are equal:

$$I_{ds\,LIN\,nmos} = I_{ds\,SAT\,pmos}$$

V_{gs} of PMOS / for PMOS

$$\beta_{pd}\left(V_{DD} - V_{Tn} - \frac{V_{OL}}{2}\right)V_{OL} = \frac{\beta_{pu}}{2}\left(-V_{DD} - V_{TP}\right)^2$$

$$\beta_{pd}\left(V_{DD} - V_{Tn} - \frac{V_{OL}}{2}\right)V_{OL} = \frac{\beta_{pu}}{2}\left(-V_{DD} + V_{Tn}\right)^2$$

$$\beta_{pd}(V_{DD} - V_T)V_{OL} - \frac{V_{OL}^2}{2}\beta_{pd} = \frac{\beta_{pu}}{2}(V_{DD} - V_T)^2$$

$$\beta_{pd}V_{OL}^2 + 2\beta_{pd}(V_{DD} - V_T)V_{OL} + \beta_{pu}(V_{DD} - V_T)^2 = 0$$

Like $ax^2 + bx + c = 0$ $\quad x_{1,2} = -\frac{b}{2a} \pm \sqrt{\frac{b^2}{4a^2} - \frac{c}{a}}$

$$V_{OL} = (V_{DD}-V_T) \pm \sqrt{(V_{DD}-V_T)^2 - \frac{\beta_{pu}}{\beta_{pd}}(V_{DD}-V_T)^2}$$

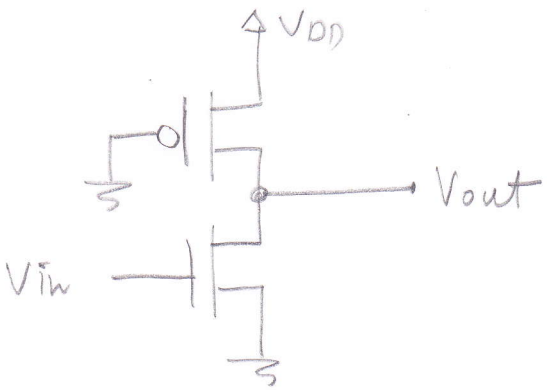
$$V_{OL} = (V_{DD}-V_T)\left[1 \pm \sqrt{1-\frac{\beta_{pu}}{\beta_{pd}}}\right]$$

↓ Only one of the solutions is valid. We need V_{OL} is low. So the valid solution which gives V_{OL} lower is:

$$V_{OL} = (V_{DD}-V_T)\left[1 - \sqrt{1-\frac{\beta_{pu}}{\beta_{pd}}}\right]$$

---

(26) For the circuit given below



$\frac{W_n}{L_n}$?

$\beta_{pd} = \left(60\ \frac{\mu A}{V^2}\right) \times \left(\frac{2.0\ \mu m}{0.5\ \mu m}\right) = 0.24\ mA/V^2$

$\beta_{pu} = \left(24\ \frac{\mu A}{V^2}\right) \times \left(\frac{0.5\ \mu m}{0.5\ \mu m}\right) = 24\ \mu A/V^2$

$V_{DD} = 5V$, $V_T = 1V$

and $V_{in} = V_{DD} = 5V$

Calculate the following:

a) The static current Istat
b) The ON-resistance of the nMOS transistor ($R_{pd\,ch}$)
c) V_{OL}
d) The static power dissipated by the inverter
e) The on-resistance of the pMOS transistor ($R_{pu\,ch}$)
f) Assume that the inverter is used to drive a capacitive load of 70×10^{-15} F. Calculate the low-to-high and high-to-low propagation delays.

SOL: a) when $V_{in} = V_{DD}$ nMOS is LIN, pMOS is SAT.

The current is determined (limited by the pMOS, since it is in SAT region, its current stays constant).

$$I_{stat} = \frac{\beta_{pu}}{2}(V_{DD}-V_T)^2 = \frac{24\times10^{-6}}{2} \times (5-1)^2 = \frac{24\times16\times10^{-6}}{2}$$

$$I_{stat} = 192\times10^{-6}\,A = 0.192\,mA$$

b) $R_{ch\,pd} = \frac{\partial V_{ds}}{\partial I_{ds}} = \frac{1}{\frac{\partial I_{ds}}{\partial V_{ds}}} = \frac{1}{\frac{\partial}{\partial V_{ds}}\left(\beta_{pd}\left(V_{DD}-V_T-\frac{V_{ds}}{2}\right)V_{ds}\right)}$ (linear region)

$= \beta_{pd}(V_{DD}-V_T) - \frac{2V_{ds}}{2} = \beta_{pd}(V_{DD}-V_T) - V_{ds} \cong \beta_{pd}(V_{DD}-V_T)$ ($V_{ds} = V_{OL}$)

$R_{ch\,pd} \cong \frac{1}{\beta_{pd}(V_{DD}-V_T)} \cong \frac{1}{0{,}24\times10^{-3}(4)} = \frac{10^3}{0{,}96}$

$\boxed{R_{ch\,pd} \cong 1{,}04\,k\Omega}$

c) $V_{OL} = (V_{DD}-V_T)\left[1-\sqrt{1-\frac{\beta_{pu}}{\beta_{pd}}}\right]$ (derived in Example 25)

$V_{OL} = (5-1)\left[1-\sqrt{1-\frac{24\times10^{-6}}{0{,}24\times10^{-3}}}\right]$ $\quad \frac{24\times10^{-6}}{24\times10^{-5}} = 10^{-1}$

$\sqrt{1-0{,}1} = \sqrt{0{,}9} \cong 0{,}95$

$V_{OL} \cong 4\,[1-0{,}95] = 4\times0{,}5 = \underline{0{,}20\,V}$

d) $P_{ST} = I_{Stat} \times V_{DD} = 192\,\mu A \times 5\,V \cong \underline{1\,mW}$

e) The PMOS transistor is operating in the SAT region (i.e. its current is constant and independent of the V_{ds})

$R_{pu_{ch}} = \frac{V_{DS}}{I_{ds}} = \frac{V_{DD}-V_{OL}}{I_{Stat}} = \frac{5V-0{,}2V}{192\times10^{-6}} \cong \underline{24.9\,k\Omega}$

f) $\boxed{t_{pLH} = \frac{1{,}7\times C}{\beta_{pu}\times V_{DD}}}$ $\qquad \boxed{t_{pHL} = \frac{1{,}7\times C}{\beta_{pd}\times V_{DD}}}$ GIVEN

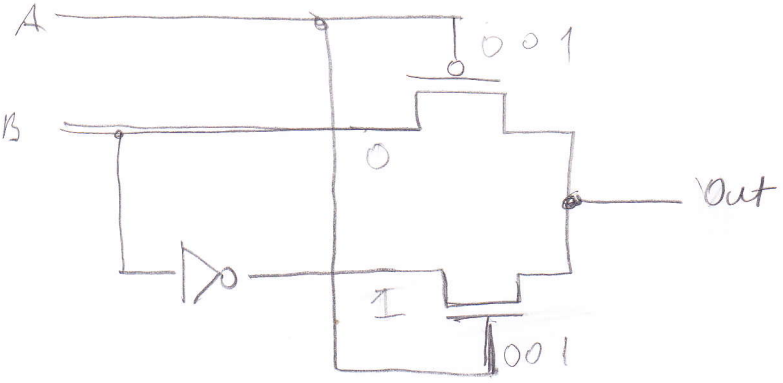
$t_{pHL} = 0{,}1\,ns$

$t_{pLH} \cong 0{,}99\,ns$

ASYMMETRY PERSISTS!

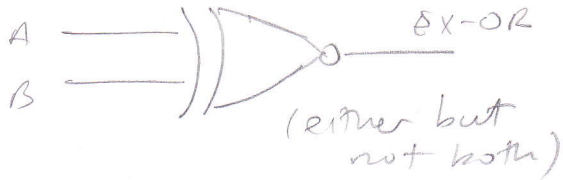
(Since in this circuit PMOS is a weak device. i.e. its β_{pu} is quite low. Therefore it can not provide the required current to charge the capacitor quickly.)

(27) What logic gate is realized by the circuit in Figure below? Does this circuit suffer from any major drawbacks?



SOL:

A	B	out
0	0	0 ($\bar{B}$)
0	1	1 (B)
1	0	1 ($\bar{B}$)
1	1	0 ($\bar{B}$)



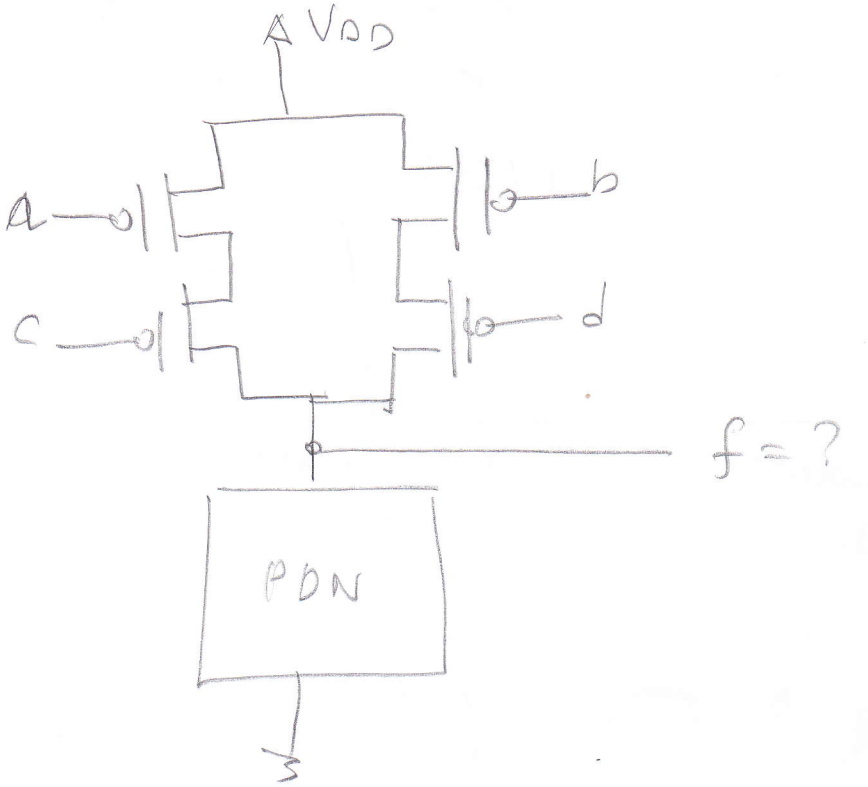
This is an EX-OR gate.

This circuit has 2 drawbacks:

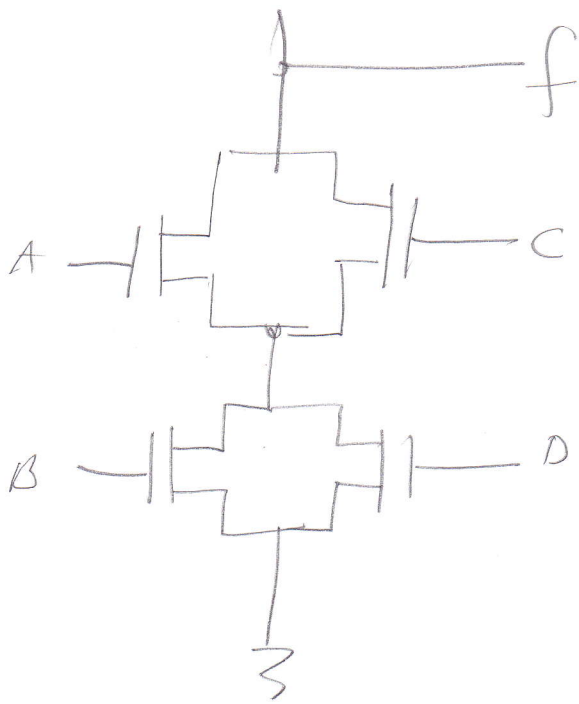
→ when both inputs are 0, the PMOS transistor must drive output to 0, resulting in OUT = V_T Volts.

→ when A = 1, and B = 0, the NMOS transistor must drive the output HIGH, resulting in OUT = $V_{DD} - V_T$

① Write the logic function of the gate



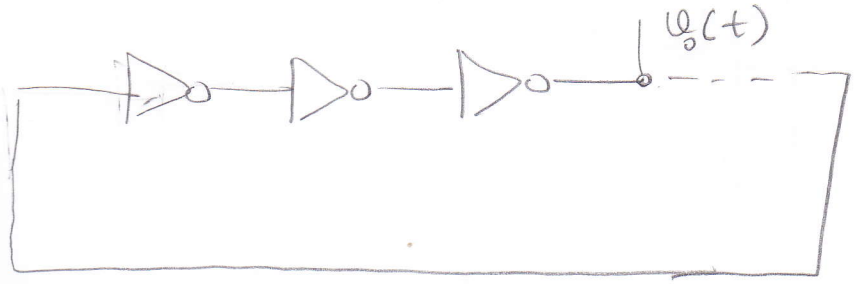
The PDN circuit:



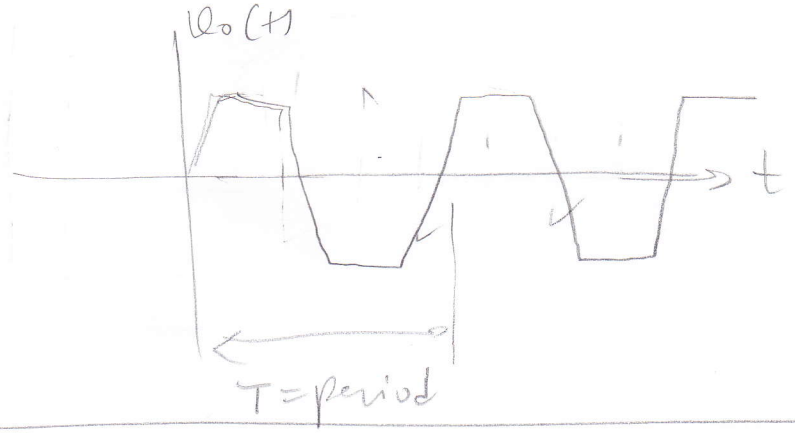
$$f = \overline{(A+C)(B+D)}$$

$$f = \bar{A}\bar{C} + \bar{B}\bar{D}$$

(2) Explain why a ring oscillator can be formed with odd numbers of inverters, but not with even numbers of inverters.



A ring counter of $2n+1$ number of inverters, where $n = 0, 1, 2, \cdots$



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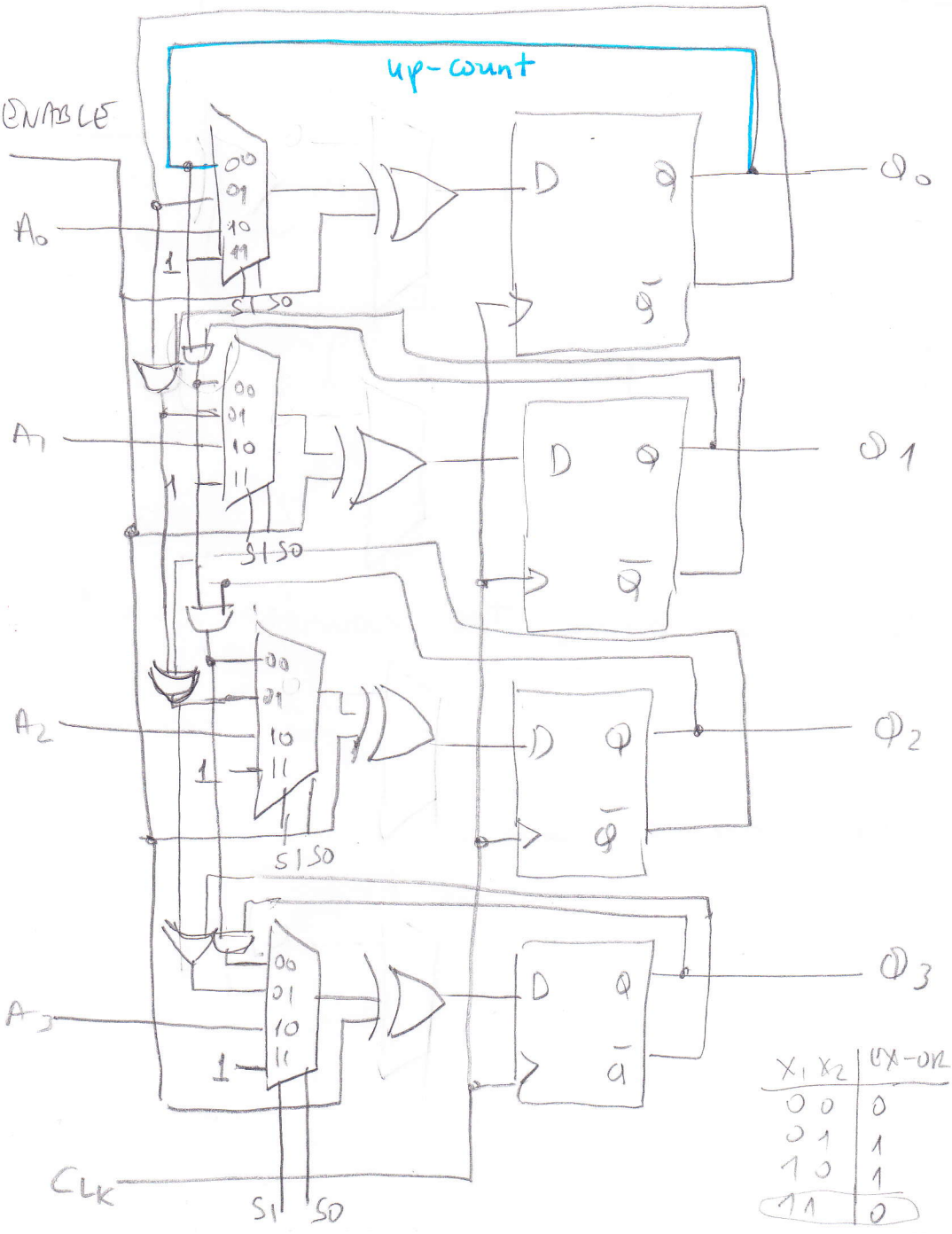
(4) Draw the stick diagram of a NAND gate with CMOS transistors.

A - DFF COUNTER WITH PARALLEL LOAD, RESET, UP AND DOWN COUNT CAPABILITY

QUESTION: Design a binary sequential counter with 4 D FFs (positive edge-triggered) that can up and down count with count_up, count_down selection of signals; The counter could be loaded with a 4-digit nbinbary number (A0 A1 A2 A3) with a LOAD selection, and all the outputs of D FFs (Q_0, Q_1, Q_2, Q_3) could be resetted with a proper selection. Use 4 multiplexers of 4 to 1 in your design. The count is started with an ENABLE command. (Enable=0 count, Enable=1 do not count)

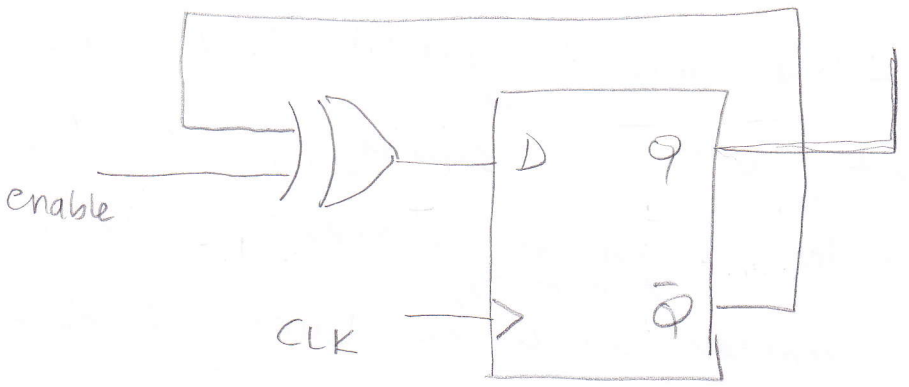


AND gates' outputs could be ONE when all inputs are ONE, which carries the previous Q value to the next D-Flip Flop for up counting, OR gates' outputs could be ZERO when all inputs are ZERO, which carries the previous Q value to the next D-Flip Flop for Down-counting

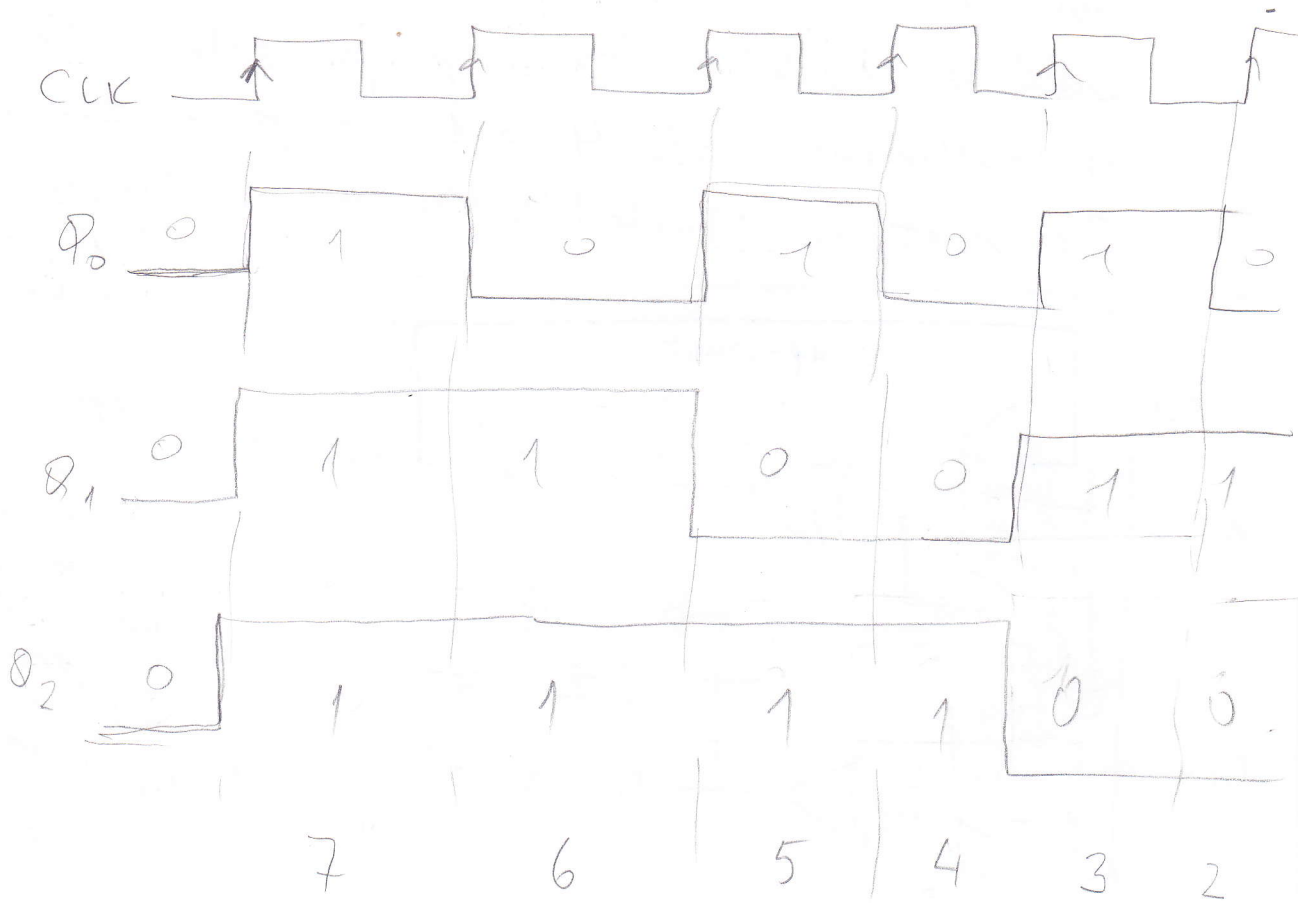
S1	S0	
0	0	Count-up
0	1	count-down
1	0	Load A
1	1	Reset

X_1	X_2	EX-OR
0	0	0
0	1	1
1	0	1
1	1	0

A DFF with DOWN COUNT CONFIGURATION

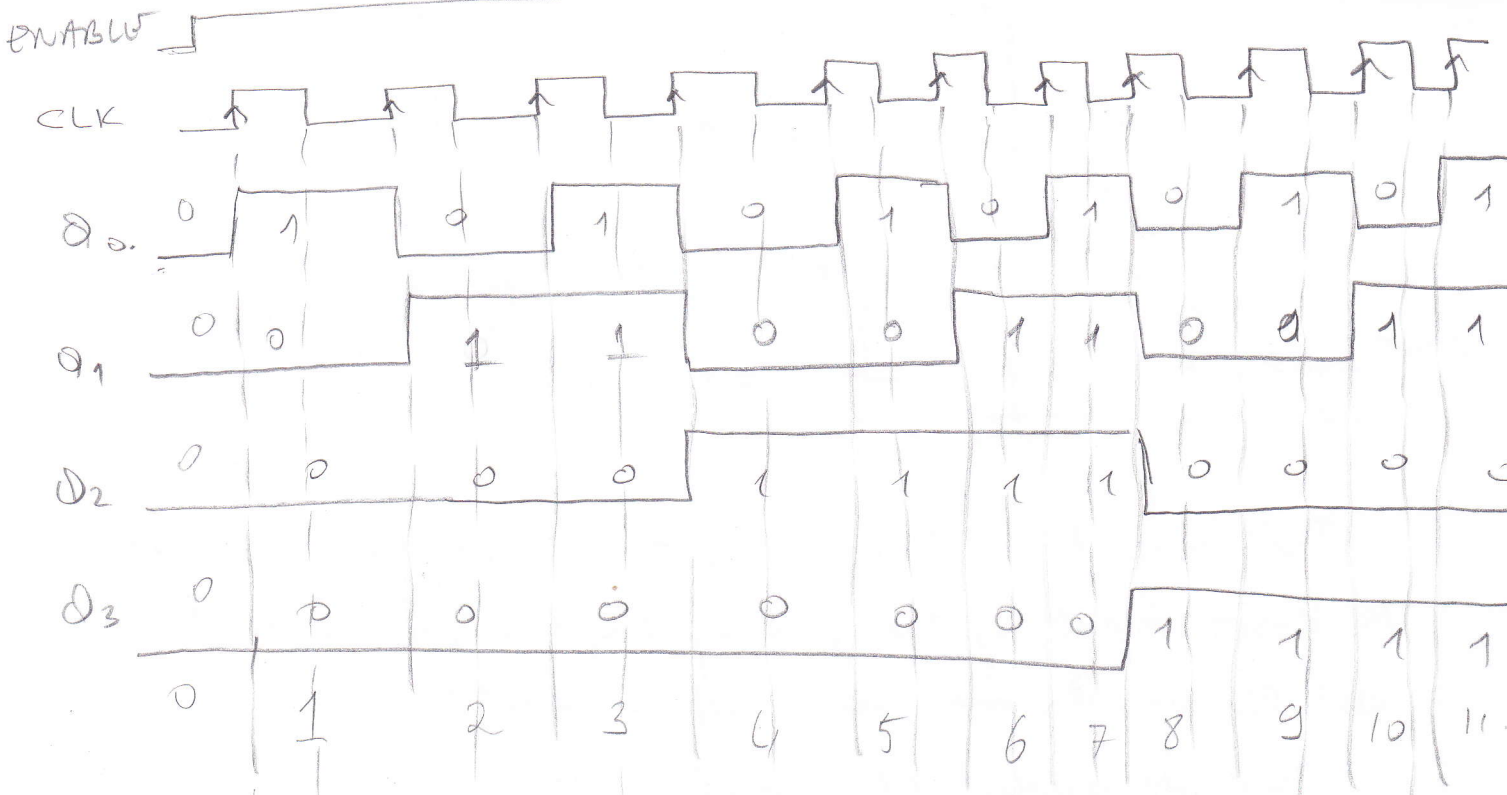


Enable	Q_n	Q_{n+1}
0	0	0 Q_n
0	1	1 Q_n
1	0	
1	1	



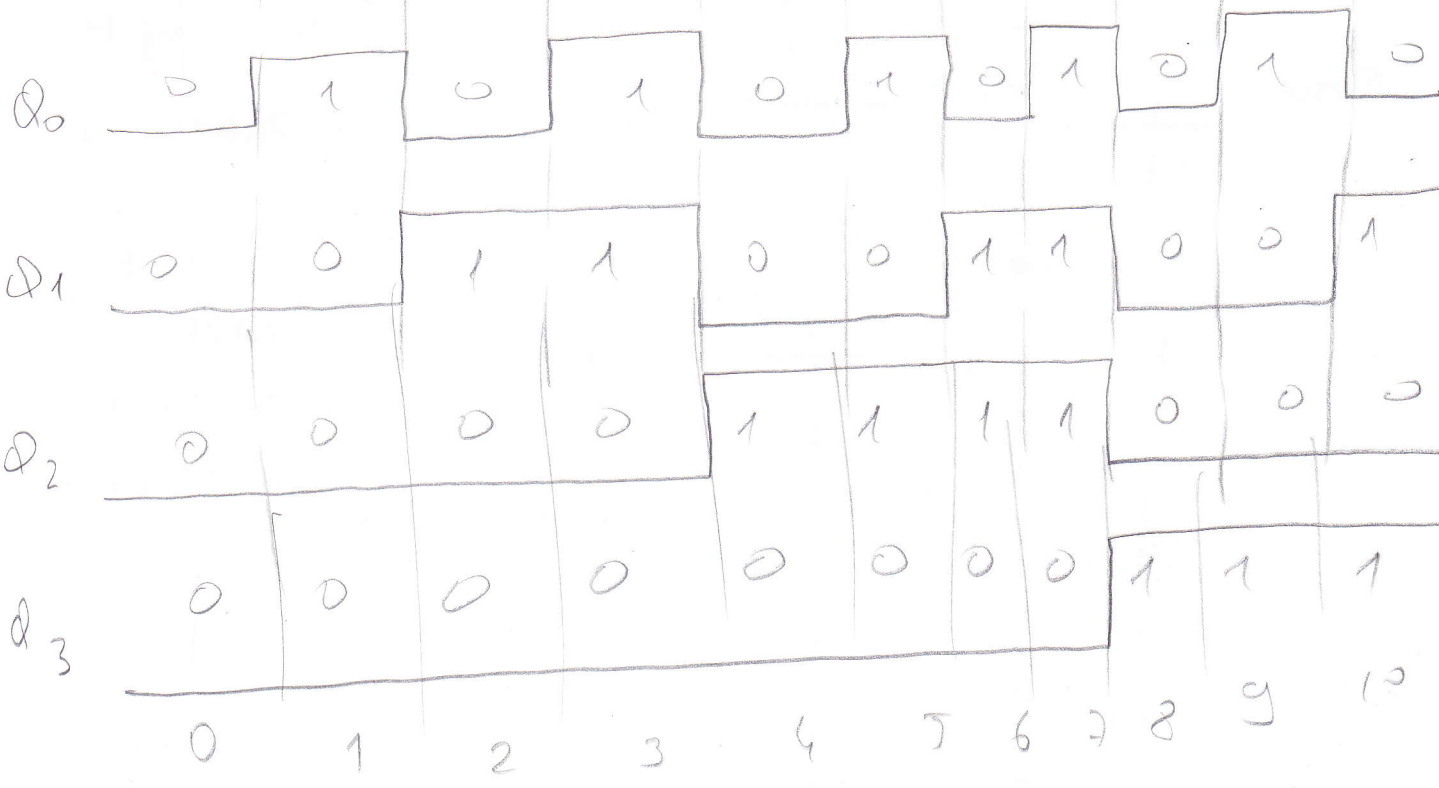
When connected This way The counter counts down.

It counts when enable = 1.

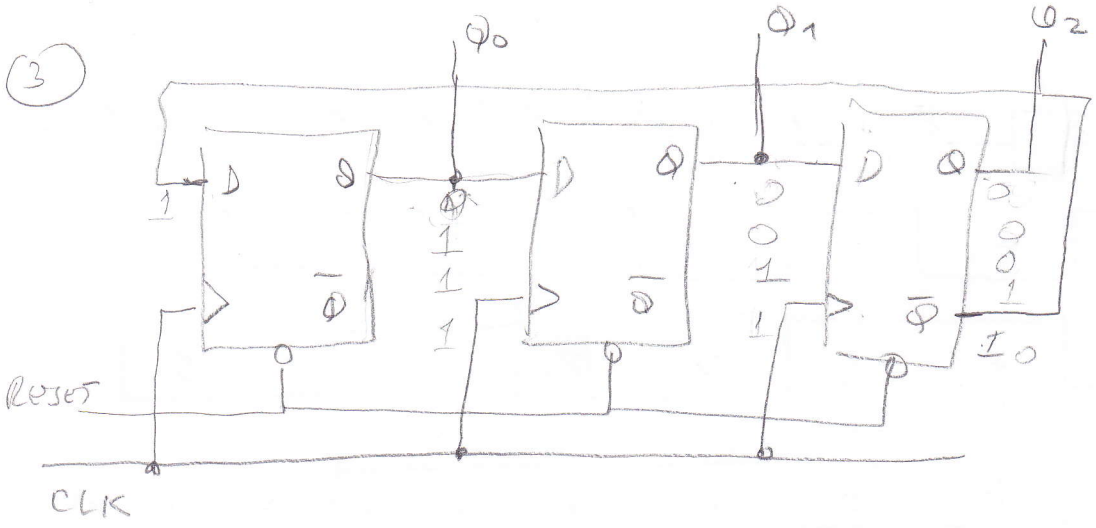


* Binary Up Counter.

If the D FF's were negative edge-triggered (i.e. ▷ in the clock) Then the counting would be



Binary Up-Counter



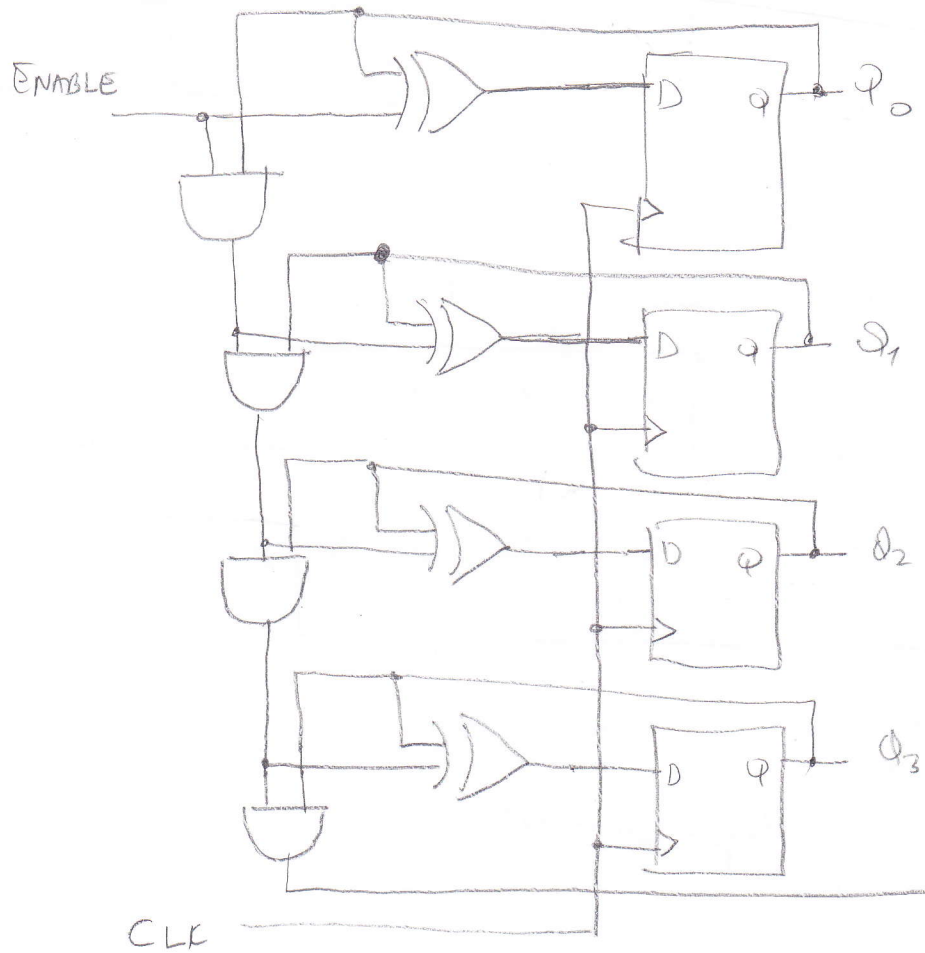
note: (Johnson Counter)

This circuit is first RESET by applying a zero to Reset inputs of the D-Flip flops (i.e. by making all Q_0, Q_1, Q_2 zero before starting).

Then we apply clk signal. Show the output cycles of this circuit for 7 CLK cycles

(Output = $Q_2 Q_1 Q_0$)

A-FOUR BIT COUNTER WITH D-FLIP FLOPS (Synchronous Counters with D-Flip Flops)



If ENABLE = 1

then

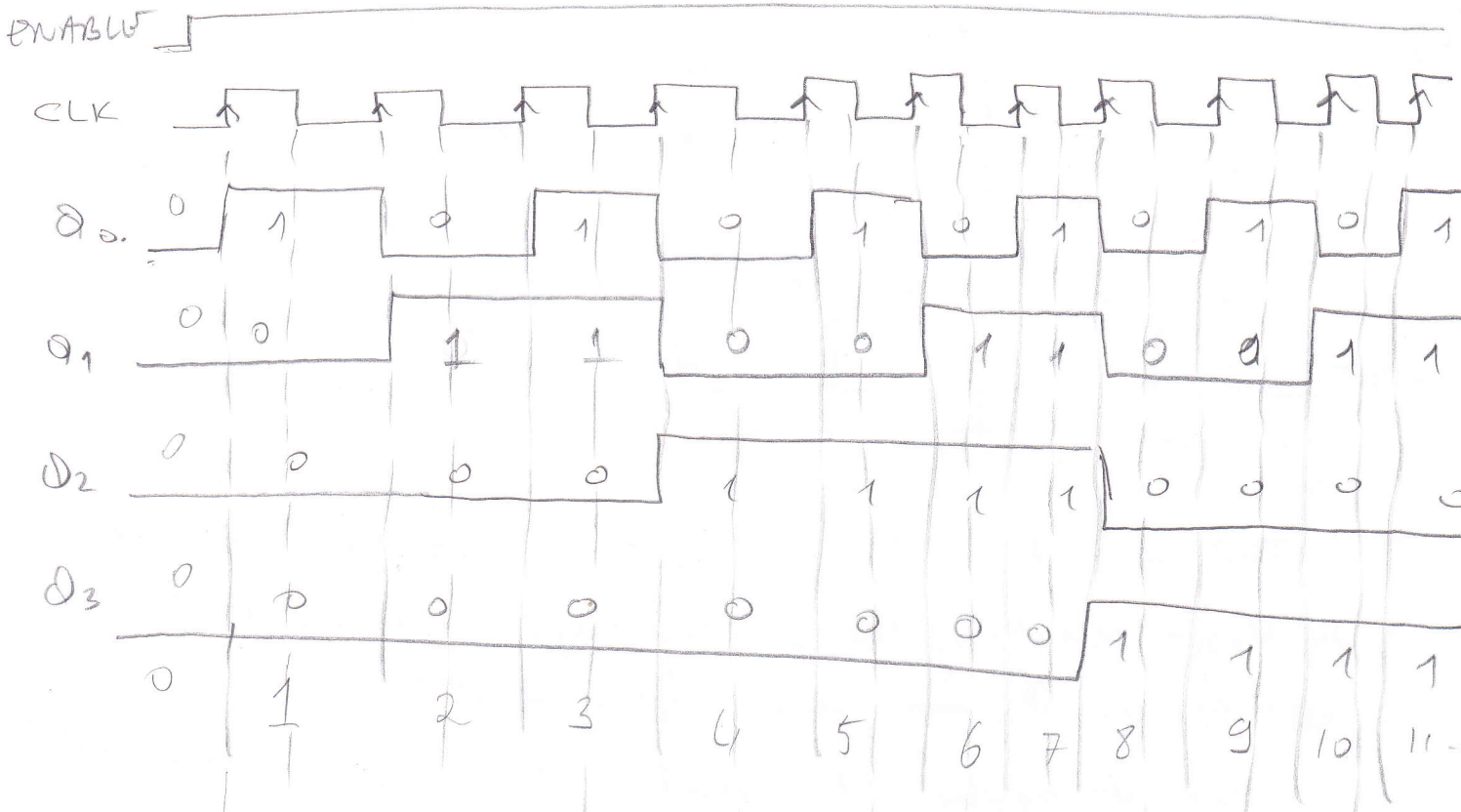
$D_0 = \overline{Q_0} = 1 \oplus Q_0$

$D_1 = Q_1 \oplus Q_0$

$D_2 = Q_2 \oplus Q_1 Q_0$

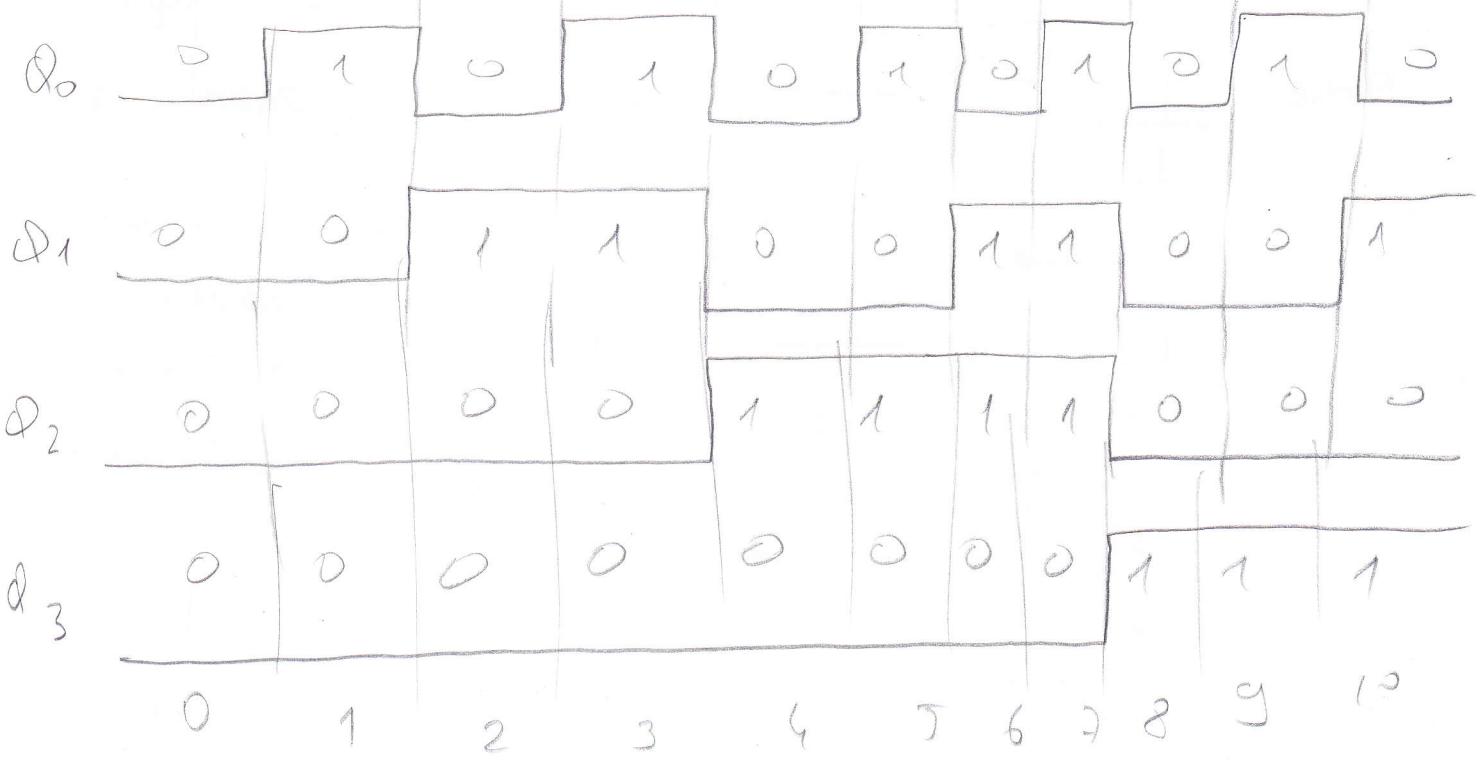
$D_3 = Q_3 \oplus Q_2 Q_1 Q_0$

COUNTING SIGNALS ⟹



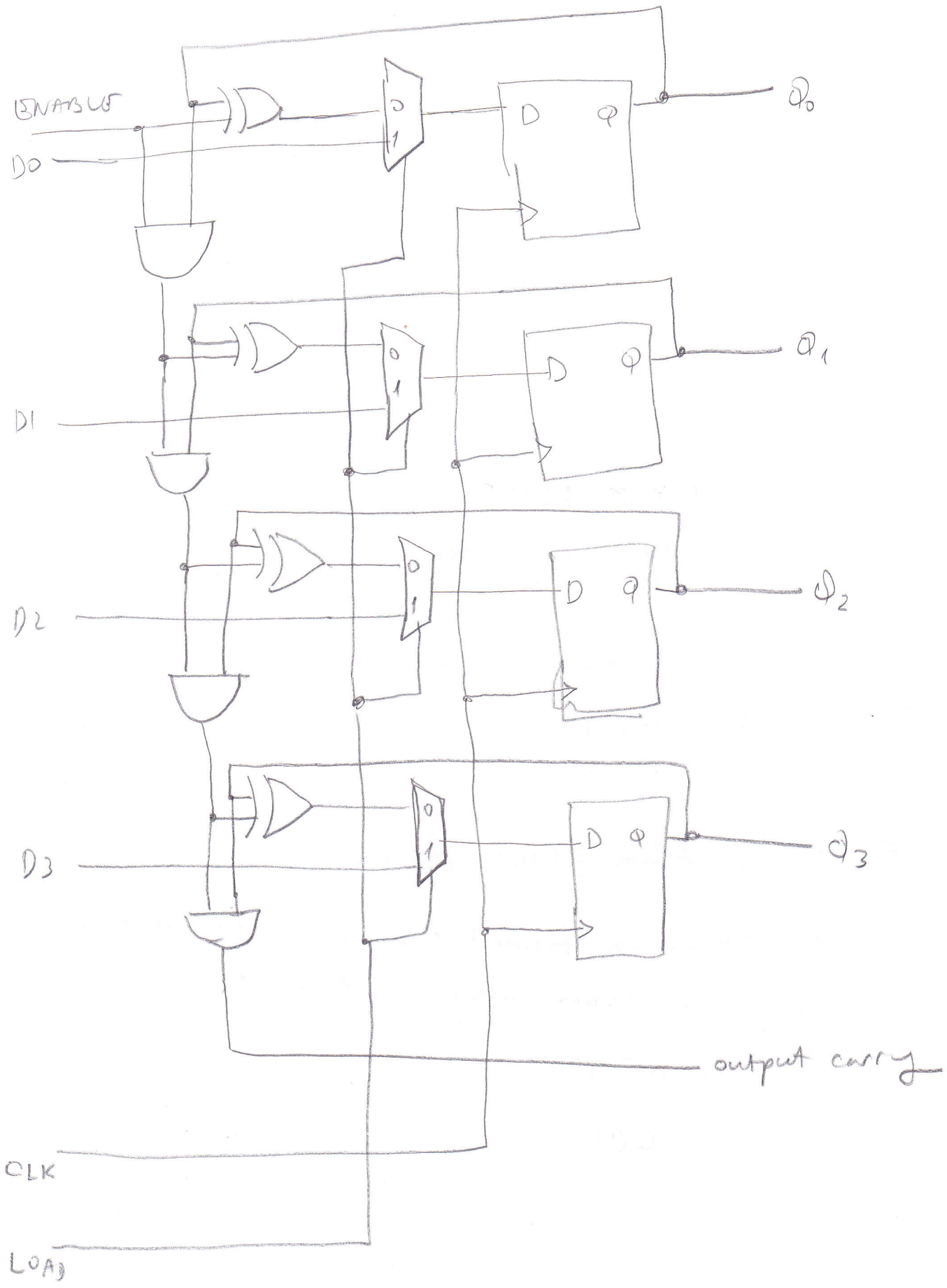
* Binary Up Counter.

If the D FF's were negative edge-triggered (i.e. ▷ in the clock) then the counting would be



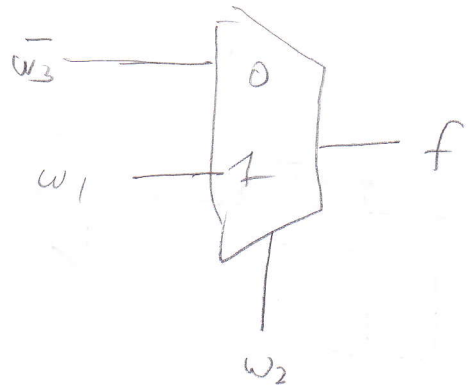
Binary Up-Counter

A - D FF Counter with parallel load capability



(6.4) $f = \bar{w}_2 \bar{w}_3 + w_1 w_2$

$f = \bar{w}_2 \bar{w}_3 + w_2 w_1$



(6.5) Solved in the book. (VHDL)

EXERCISES

SEQUENTIAL CIRCUIT

(7-13) Solved in the class (very similar)

(7.16) solved in the book.

(7.17) Use D-flip flops as:

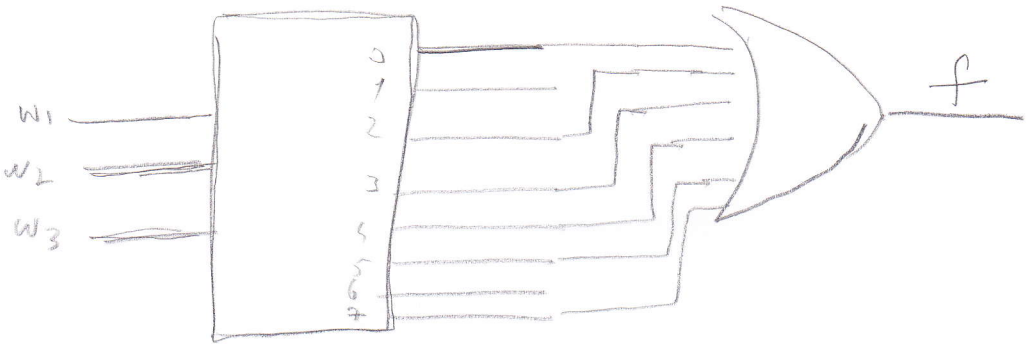
A T FF can be formed from a D-FF by providing the extra gating that gives

$$D = Q\bar{T} + \bar{Q}T$$

$$D = Q \oplus T$$

EXERCISES / COMBINATIONAL CIRCUITS

$f(w_1, w_2, w_3) = \sum m(0, 2, 3, 4, 5, 7)$



6.3

$f = \bar{w}_1 \bar{w}_3 + w_2 \bar{w}_3 + \bar{w}_1 w_2$

$= \bar{w}_1 \bar{w}_3 + (w_1 + \bar{w}_1) w_2 \bar{w}_3 + \bar{w}_1 w_2$

$= \bar{w}_1 \bar{w}_3 + w_1 w_2 \bar{w}_3 + \bar{w}_1 w_2 \bar{w}_3 + \bar{w}_1 w_2$

$= \bar{w}_1 \bar{w}_3 (1 + w_2) + w_1 w_2 \bar{w}_3 + \bar{w}_1 w_2$

$= \bar{w}_1 \bar{w}_3 + w_1 w_2 \bar{w}_3 + \bar{w}_1 w_2$

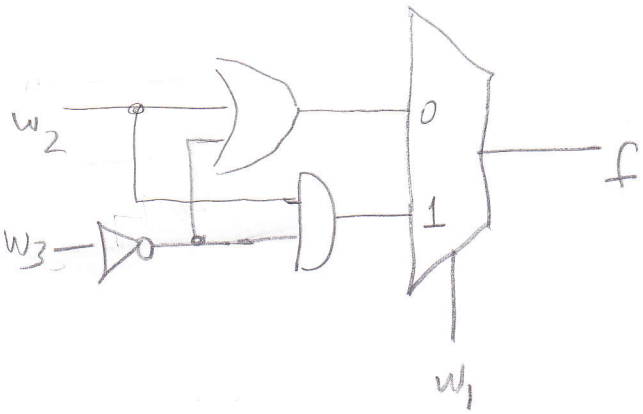
$\boxed{f = \bar{w}_1 (w_2 + \bar{w}_3) + w_1 (w_2 \bar{w}_3)}$

we need to express f in a form of

$f = w_1 f_{\bar{w}_1} + \bar{w}_1 f_{w_1}$

Shannon's Theorem

Shannon's expression



or by writing the truth table:

w_1	w_2	w_3		w_1	f
0	0	0	1	0	$w_2 + \bar{w}_3$
0	0	1	0	1	$w_2 \bar{w}_3$
0	1	0	1		
0	1	1	1		
1	0	0	0		
1	0	1	0		
1	1	0	1		
1	1	1	0		